BAT32A237 Datasheet

Ultra-low power 32-bit microcontrollers based on ARM® Cortex®-M0+

128KB Flash, analog functions, safety functions, timers and communication interfaces.

V1.0.8

Function

- **Ultra-low power operation environment:**
  - Supply voltage range: 2.0V to 5.5V
  - Temperature range: -40℃ to 125℃
  - Low power mode: sleep mode, deep sleep mode
  - Operating power consumption: 120uA/ MHz@48MHz
  - Power consumption in deep sleep mode: 0.7uA
  - Deep sleep mode +32.768K+RTC operation: 0.8uA
- **Kernel:**
  - ARM®32-bit Cortex-M0®+ CPU with MPU memory protection unit
  - Working frequency: 32KHz~48MHz
- **Memory:**
  - 128KB Flash memory, program and data storage sharing
  - 1.5KB dedicated data Flash memory
  - 12KB SRAM MEMORY WITH PARITY
- **Power and reset management:**
  - Built-in power-on reset (POR) circuit
  - Built-in voltage detection (LVD) circuit (threshold voltage settable).
- **Clock Management:**
  - Built-in high-speed vibrator, accuracy (±1%). 1MHz~48MHz system clock is available. 1MHz~64MHz peripheral module operation clock is available
  - Built-in 15KHz low-speed oscillator
  - Support 1MHz~20MHz external crystal oscillator
  - Supports 32.768KHz external crystal oscillator
- **Multiplier/ divider module:**
  - Multiplier: Supports single-cycle 32 bitmultiplication operations
  - Divider: Supports 32bit signed integer division operations, only 4 or 8 CPU clock cycles to complete the operation
- **Enhanced DMA Controller:**
  - The interrupt triggers the start.
  - Selectable transfer modes (normal transfer mode, repeated transfer mode, block transfer mode and chain transfer mode)
  - The transmission source/ destination
- **Input/ output ports:**
  - I/O ports: 29~59
  - It can switch between N-channel open drain, TTL input buffering, and internal pull-up
  - Built-in keys interrupt the checkout function
  - Control circuit with built-in clock output/ buzzer output
- **Serial two-wire debugger (SWD).**
- **Abundant timers:**
  - 16-bit timer: 9 channels with general-purpose PWM and motor-specific PWM functions
  - 15-bit interval timer: 1
  - Real-time clock (RTC): 1 (with perpetual calendar, alarm clock function, and supports a wide range of clock correction).
  - Watchdog timer (WWDT): 1pcs
  - SysTick timer
- **Rich and flexible interfaces:**
  - Two serial communication units: serial communication unit 0 can be freely configured as 2-channel standard UART or 4-channel 3-wire SPI or 4-channel simple I^2C; Serial communication unit 1 can be freely configured as 1-channel standard UART, 2-channel 3-wire SPI or 2-channel simple I^2C; (UART of unit 0 supports LIN Bus communication, SPI00 channel supports 4-wire SPI communication)
  - Standard I^2C: 1 channel
  - IrDA: 1 channel
  - CAN: 1 channel
- **Security features:**
  - Complies with IEC/ UL 60730 standards
  - An abnormal storage space access error is reported
  - Supports RAM parity
  - Support hardware CRC verification
  - Support important SFR protection to prevent misoperation
  - 128-bit unique ID number
  - Grade 2 protection of F lash in debug mode (level 1: can only be erased in all areas of flash, cannot read and write; Level 2: The emulator connection is invalid and cannot be operated on flash).

realm is selectable from the full address space range

- **Linkage controller:**
  - It can link event signals together to realize the linkage of peripheral functions
  - There are 22 types of event input and 10 types of event triggering
- **Rich analog peripheral:**
  - 12-bit precision ADC converter with 1.06msps conversion rate, 16 external analog channels with temperature sensor support for single-channel conversion mode and multi-channel sweep conversion mode. Conversion range: 0 to positive reference voltage
  - 8-bit precision D/ A converter, 1 or 2 channel analog output, real-time output function, output voltage range 0~V_{DD}
  - Comparator (CMP) with built-in two-channel comparator with selectable input source and selectable reference voltage external or internal reference
  - Programmable gain amplifier (PGA) with built-in two-channel PGA programmable 4/ 8/ 10/ 12/ 14/ 16/ 32x gain with an external GND pin .
- **Package:**
  - Support 24Pin~64Pin in a variety of package forms

1 Overview

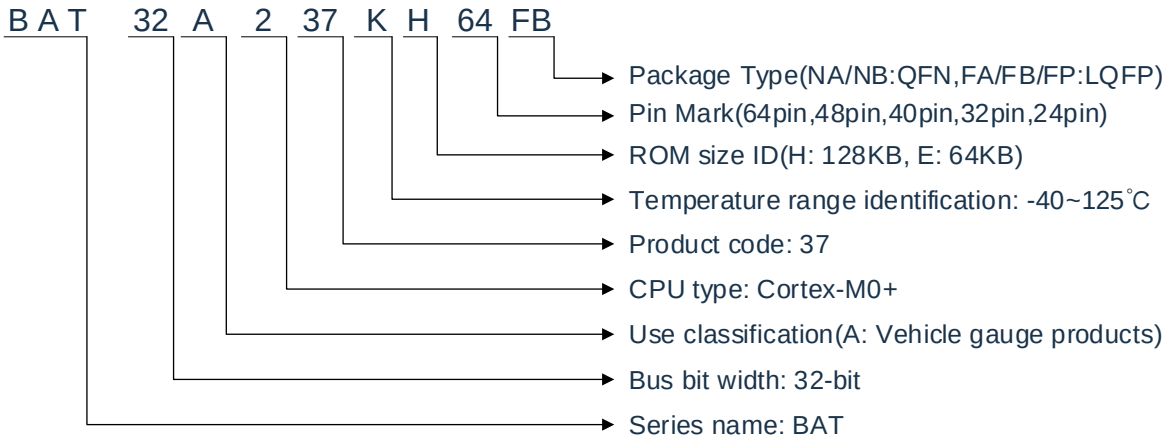
1.1 Brief Introduction

BAT32A237 series conforms to AEC-Q100 Grade1 automotive product standard, -40~125℃ working environment temperature, supports 24~64Pin in a variety of QFN, LQFP packages. This product uses the high-performance ARM Cortex-M0®+ 32bit RISC core, which can operate at up to 48 MHz. High-speed embedded flash memory (the maximum SRAM is 12KB, and the maximum program/ data flash memory is 128KB). This product integrates I^2C, SPI, UART, LIN, CAN bus and other standard interfaces, integrated 12bit A/ D converter, temperature sensor, 8bit D/ A converter, comparator, programmable gain amplifier. The 12bit A/ D converter can be used to acquire external sensor signals to reduce system design cost. The 8bit D/ A converter can be used for audio playback or power control. An integrated temperature sensor enables real-time monitoring of the external ambient temperature. An integrated comparator can be used in applications such as motor control feedback or battery monitoring. Integrate a variety of advanced timer modules, load 1-channel SysTick timer, 17-channel 16bit timer, 1-channel 15bit interval timer, watchdog timer and real-time clock and other functions, It can also support applications such as general-purpose PWM and motor-specific PWM.

The BAT32A237 also has excellent low-power performance, supporting both sleep and deep sleep modes for design flexibility. It consumes 120uA/ MHz@48MHz and consumes only 0.7uA in deep sleep mode. At the same time, due to the integrated event linkage controller, direct connection between hardware modules can be realized without CPU intervention, which is faster than using interrupts.

The BAT32A237 microcontroller family's excellent reliability, rich integrated peripheral functions, and excellent low-power performance make it suitable for a wide range of automotive product development.

1.2 Product Model List



Product List for BAT32A237:

Number of pins	package	Product model
24pins	24-pin plastic package LQFP (4x4mm, 0.5mm pitch)	BAT32A237KE24NA
32 pins	32-pin plastic package LQFP (7x7mm, 0.8mm pitch)	BAT32A237KH32FP
40 pins	40-pin plastic package QFN (5x5mm, 0.4mm pitch)	BAT32A237KH40NB
48 pins	48-pin plastic package LQFP (7x7mm, 0.5mm pitch)	BAT32A237KH48FA
64 pins	64-pin plastic package LQFP (7x7mm, 0.4mm pitch)	BAT32A237KH64FB

FLASH, SRAM CAPACITY:

Flash memory	Specific data Flash memory	SRAM	BAT32A237		
			24 pins	32 pins	40 pins
64/128KB	1.5KB	12KB	BAT32A237KE24NA	BAT32A237KH32	BAT32A237KH40

Flash memory	Specific data Flash memory	SRAM	BAT32A237	
			48 pins	64 pins
128KB	1.5KB	12KB	BAT32A237KH48	BAT32A237KH64

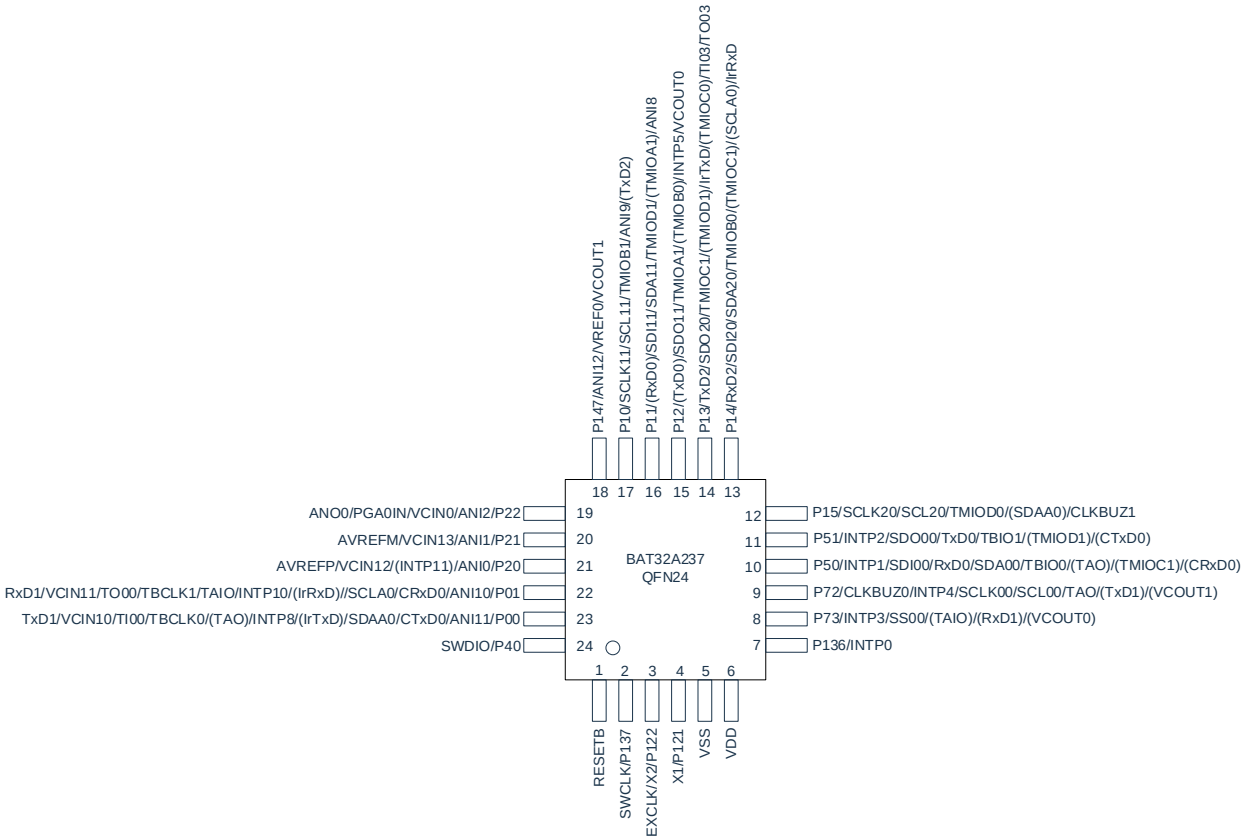
Product Selection Table for BAT32A237:

Part No.	kernel	Clock speed (MHz)	Minimum operating voltage (V).	Maximum operating voltage (V).	Code Flash (KB)	SRAM (KB)	Data Flash (KB)	D MA	GPIO	12bit ADC	8bit DAC	Comparator CMP	Amplifier PGA	General-purpose timer (16bit).	Real-time clock (RTC).	Watchdog timer (WDT).	Asynchronous serial bus (UART).	Synchronous serial bus (SPI).	IC bus	IrDA bus	LIN bus	CAN bus	Hardware multiplier	Hardware divider	Package
BAT32A237 KE24NA	M0+	48	2.0	5.5	64	12	1.5	35	21	8+3	1	2	1	9	1	1	3	3	1+3	1	1	1	Y	Y	QFN 24
BAT32A237 KH32FP	M0+	48	2.0	5.5	128	12	1.5	35	29	10+3	2	2	1	9	1	1	3	3	1+3	1	1	1	Y	Y	LQFP 32
BAT32A237 KH40NB	M0+	48	2.0	5.5	128	12	1.5	36	37	12+4	2	2	2	9	1	1	3	4	1+4	1	1	1	Y	Y	QFN 40
BAT32A237 KH48FA	M0+	48	2.0	5.5	128	12	1.5	36	45	15+4	2	2	2	9	1	1	3	5	1+5	1	1	1	Y	Y	LQFP 48
BAT32A237 KH64FB	M0+	48	2.0	5.5	128	12	1.5	37	59	16+4	2	2	2	9	1	1	3	6	1+6	1	1	1	Y	Y	LQFP 64

1.3 Top View

1.3.1 BAT32A237KE24NA

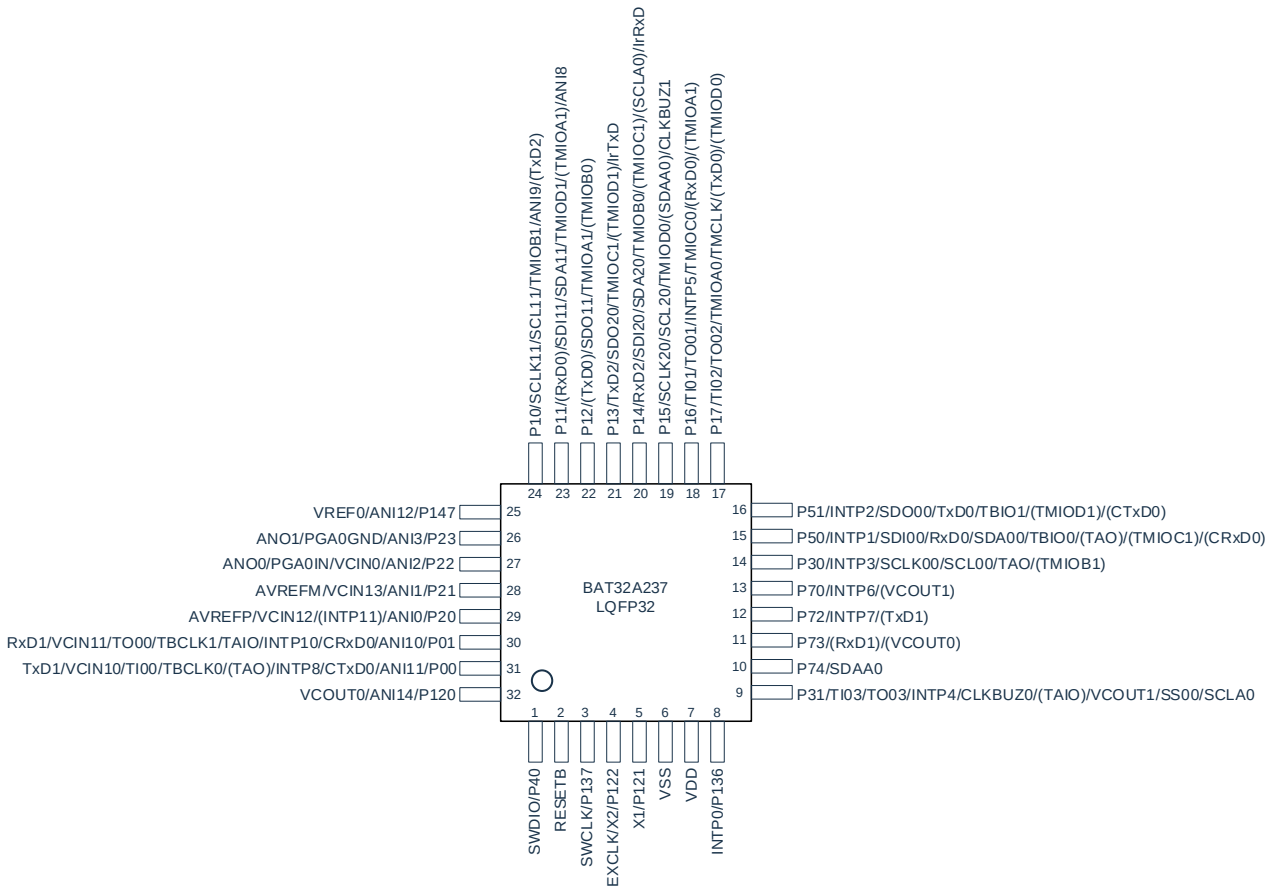
• 24-pin plastic QFN(4x4mm、0.5mm pitch)



Note: The functions in () of the above Figure can be assigned by setting the peripheral I/ O redirection registers.

1.3.2 BAT32A237KH32FP

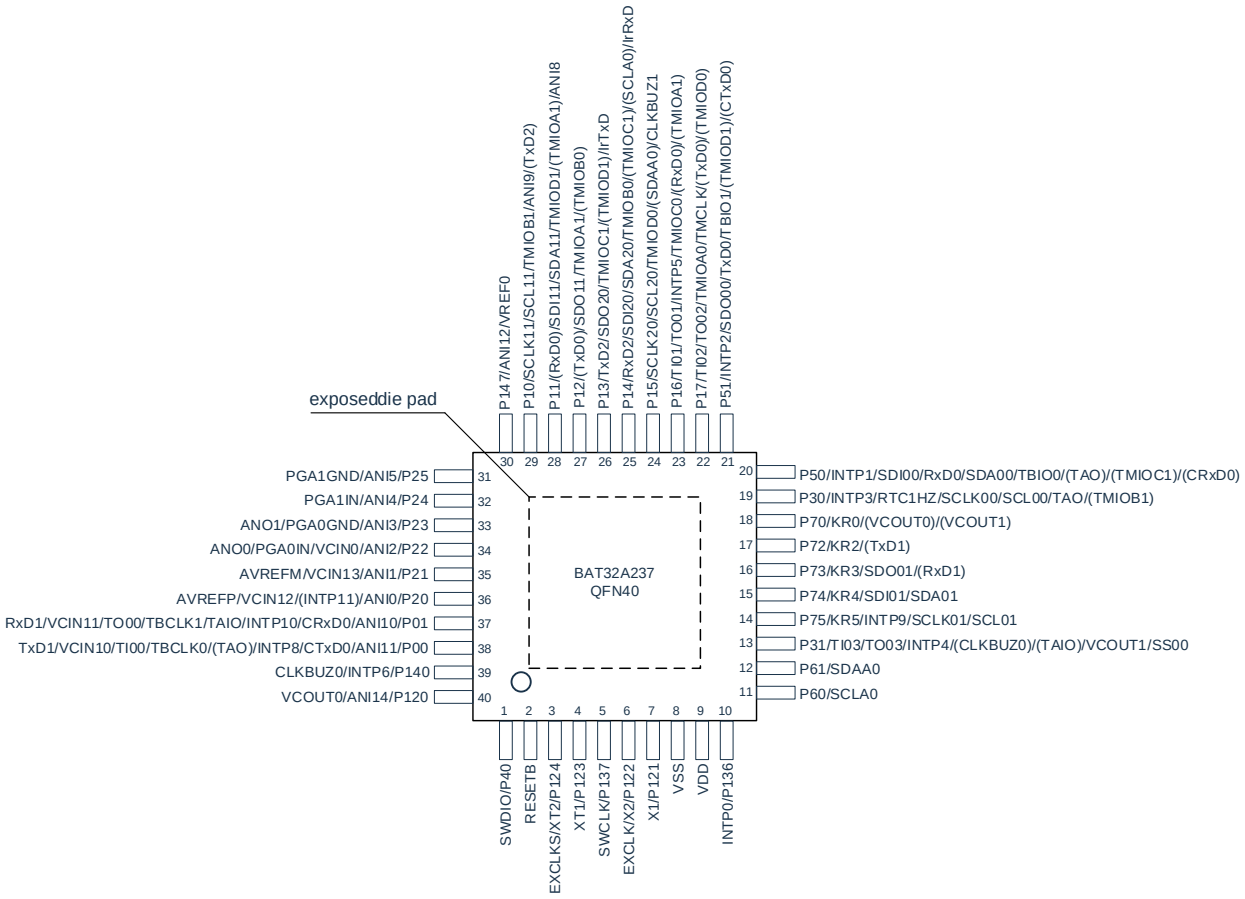
• 32-pin plastic LQFP (7x7mm, 0.8mm pitch).



Note: The functions in () of the above Figure can be assigned by setting the peripheral I/ O redirection registers.

1.3.3 BAT32A237KH40NB

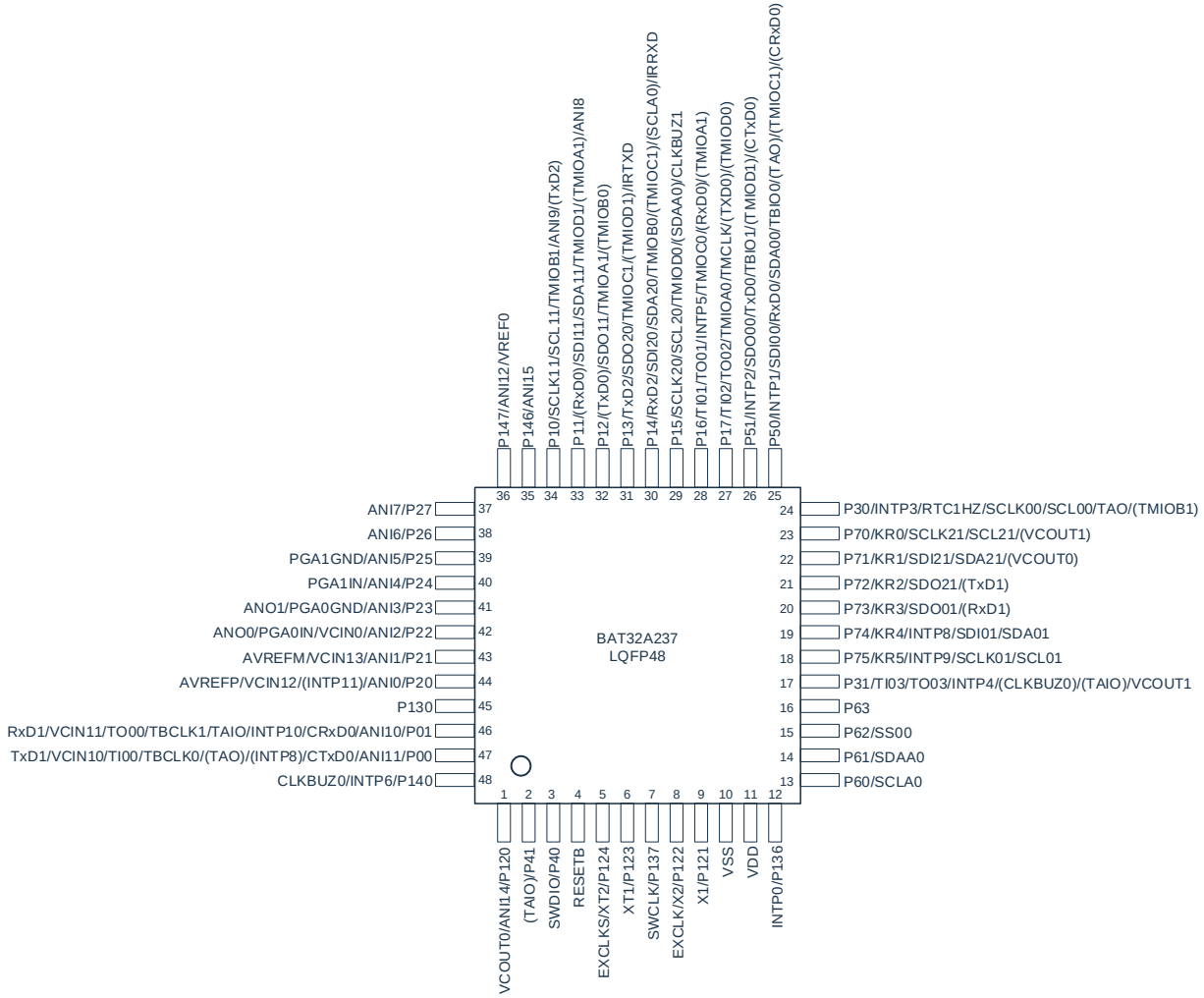
• 40-pin plastic QFN (5x5mm, 0.4mm pitch).



Note: The functions in () of the above Figure can be assigned by setting the peripheral I/ O redirection registers.

1.3.4 BAT32A237KH48FA

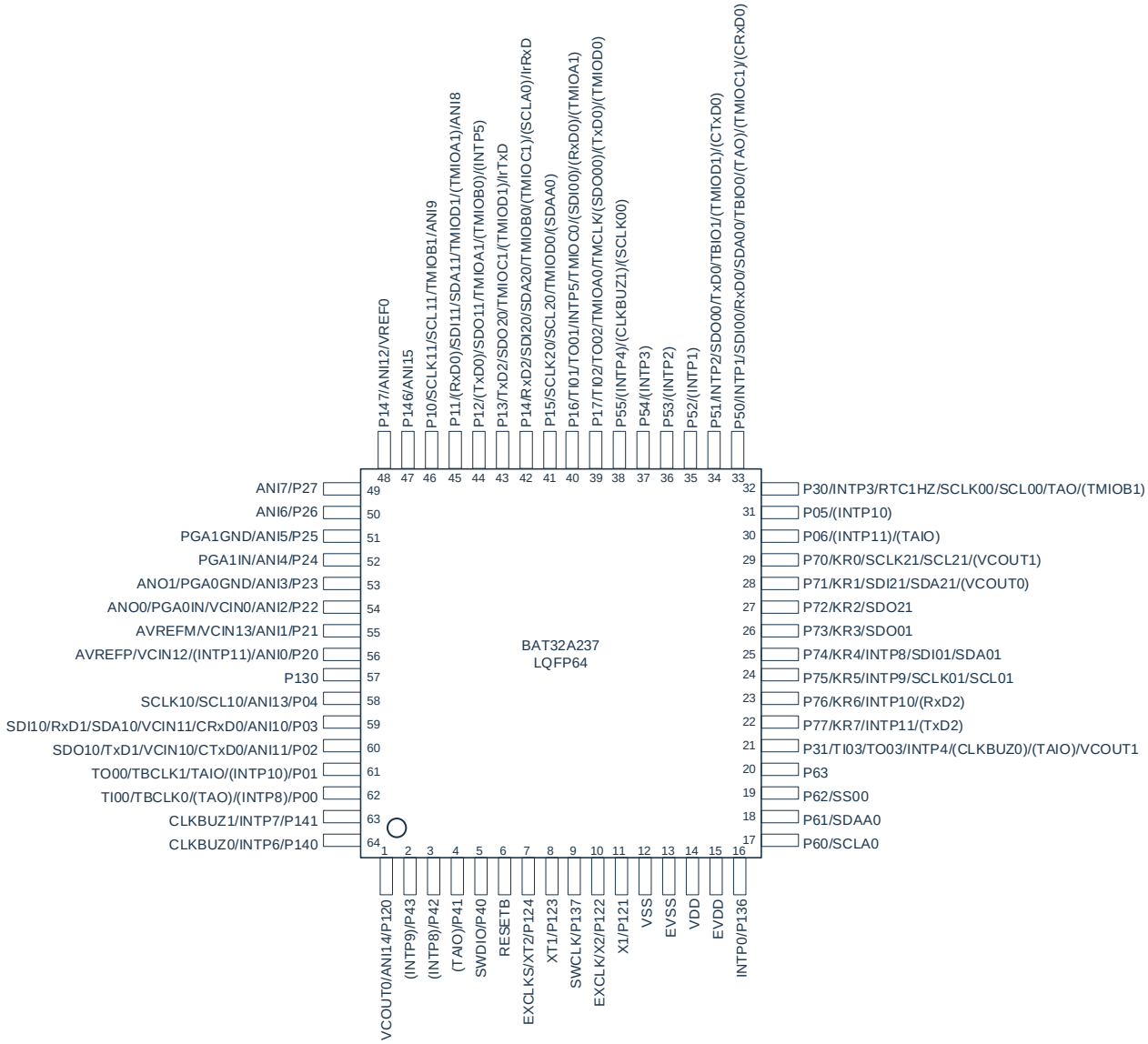
• 48-pin plastic LQFP (7x7mm, 0.5mm pitch).



Note: The functions in () of the above Figure can be assigned by setting the peripheral I/ O redirection register.

1.3.5 BAT32A237KH64FB

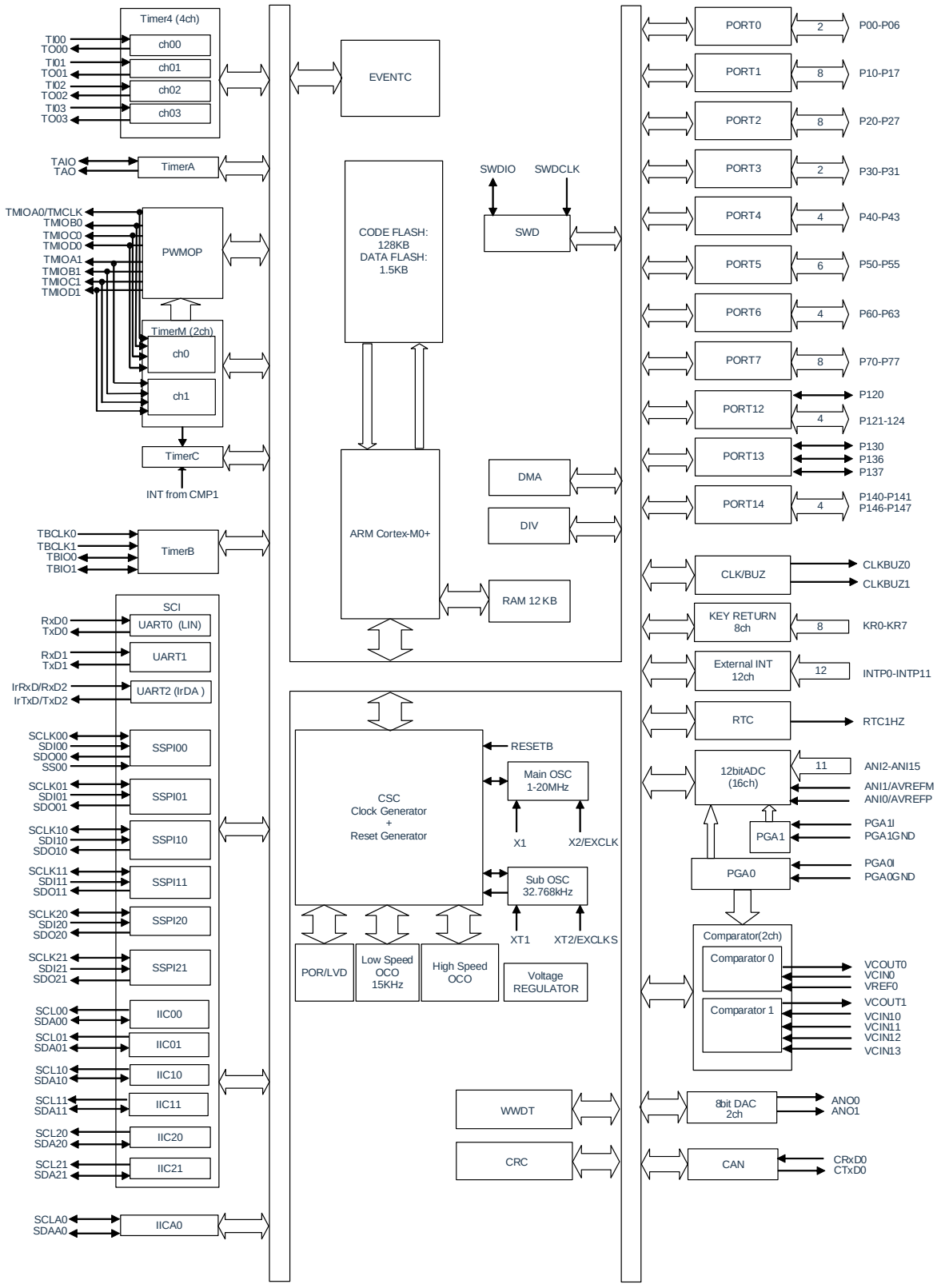
• 64-pin plastic LQFP (7x7mm, 0.4mm pitch).



Note:

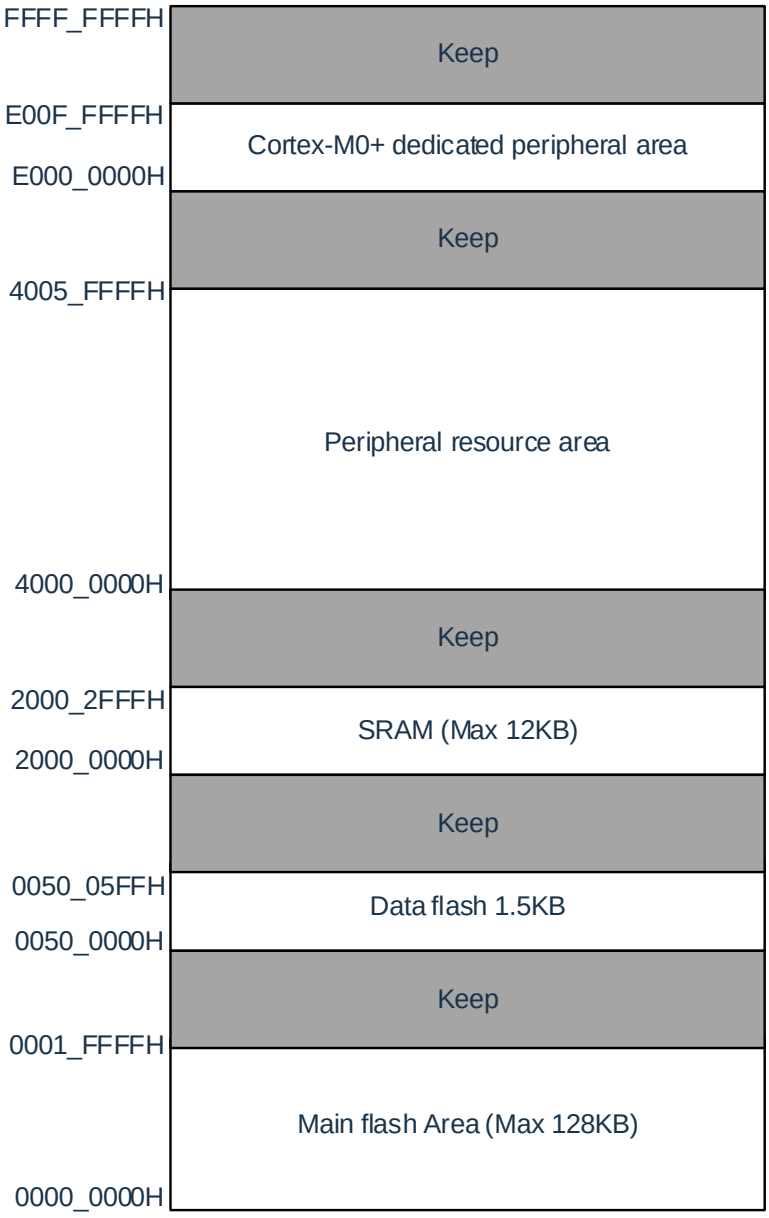
1. The EV_{SS} pin and V_{SS} pin must be the same potential.
2. The voltage at the V_{DD} pin must be equal to the voltage at the EV_{DD} pin.
3. In the case where it is necessary to reduce the noise generated from the MCU in the application field, it is recommended to take noise countermeasures such as providing power to V_{DD} and EV_{DD} separately and grounding V_{SS} and EV_{SS} separately.
4. The functions in () of the above Figure can be assigned by setting the peripheral I/ O redirection registers.

2 Product Structure Diagram



Note: The figure above is a block diagram of a 64-pin product, and some functions of products below 64-pin are not supported.

3 Memory Map


FFFF_FFFFH
Keep
E00F_FFFFH
Cortex-M0+ dedicated peripheral area
E000_0000H
Keep
4005_FFFFH
Peripheral resource area
4000_0000H
Keep
2000_2FFFH
SRAM (Max 12KB)
2000_0000H
Keep
0050_05FFH
Data flash 1.5KB
0050_0000H
Keep
0001_FFFFH
Main flash Area (Max 128KB)
0000_0000H

4 Pin Function

4.1 Port Functionality

The relationship between the power supply and the pins is shown below

64-pin product:

Power/ Ground	The corresponding pin
EV_{DD}/ EV_{SS}	• Port pins other than P20~P27, P121~P124, P137 and RESETB
V_{DD}/ V_{SS}	• P20~P27, P121~P124, P137 and RESETB

Products other than 64pins use a single power supply, and all pins are powered by V_{DD}.

All ports of this product are divided into 5 types according to type, which are type1~type5, and the corresponding situation is as follows:

Type 1: Bidirectional I/ O capability

Type 2: NOD function, corresponding to pins P60-P63

Type 3: Only input functions, such as clocks, correspond to pins P121-P124

Type 4: Only output function, corresponding to pin P130

Type 5: RESET function, corresponding to pin RESETB

The leadframe diagram of each type is detailed in 4.3 Port Types

4.1.1 24pin Product Pin Function Description

Function name	Port type	Input/ Output	After the reset is released	Multplexing features	Function
P00	Type 1	Input/ Output	Input port	ANI11/TxD1/VCIN10/TI00/TBCLK0/（TAO）/（INTP8）/IrTxD/SDAA0/CTxD0	Port 0 3-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The input of P01 can be set to TTL input buffer. The output of P00 can be set to an N-channel open-drain output (V_{DD} withstand voltage).
P01				ANI10/RxD1/VCIN11/TO00/TBCLK1/TAIO/（INTP10）/IrRxD/SCLA0/CRxD0	
P06				SCLK11/SCL11/TMIOB1/ANI9/(TxD2)	
P10		Input/ Output	Analog function	（RxD0）/SDI11/SDA11/TMIOD1/（TMIOA1）/ANI8	Port 1 3-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The inputs of P10 can be set to TTL Input buffering. The outputs of P10 and P11 can be set to N-channel open-drain output (V_{DD} withstand voltage). P10 and P11 can be set as analog inputs.
P11				（TxD0）/SDO11/TMIOA1/（TMIOB0）/（INTP5）/VCOUT0	
P12			Input port	TxD2/SDO20/TMIOC1/（TMIOD1）/IrTxD/TI03/TO03	
P20		Input/ Output	Analog function	RxD2/SDI20/SDA20/ TMIOB0/（TMIOC1）/（SCLA0）/IrRxD	Port 2 3-bit input/ output ports that can be specified as inputs or outputs in bits. Can be set as an analog input.
P21				SCLK20/SCL20/TMIOD0/（SDAA0）/CLKBUZ1	
P22				ANI0/AVREFP/VCIN12/（INTP11）	
P30		Input/ Output	Input port	ANI1/AVREFM/VCIN13	Port 3 1-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The input of P30 can be set to TTL input buffering. The output of P30 can be set to N-channel open-drain output (V_{DD} withstand voltage).
P40		Input/ Output	Input port	ANI2/ANO0/PGA0IN/VCIN0	Port 4 1-bit input/ output port, can be specified as input or output. The input port can be set by software using internal pull-up resistors.
P50		Input/ Output	Input port	SWDIO	Port 5 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The input of the P50 can be set to TTL input buffer. The outputs of the P50 and P51 can be set to an open-drain output of the N-channel (V_{DD} withstand voltage).
P51				INTP1/SDI00/RxD0/SDA00/TBIO0/（TAO）/（TMIOC1）/（CRxD0）	
P71		Input/ Output	Input port	INTP2/SDO00/TxD0/TBIO1/（TMIOD1）/（CTxD0）	Port 7 3-bit input/ output ports that can be

P72				CLKBUZ0/INTP4/SCLK00/SCL00/TAO/(TxD1)/(VCOUT1)	specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. (V_{DD} withstand voltage).
P73				INTP3/SS00/(TAIO)/(RxD1)/(VCOUT0)	
P121	Type 3	Input	Input port	X1	Port 12 2-bit input/ output port
P122				X2/EXCLK	
P136	Type 1	Input/ Output	Input port	INTP0	Port 13 2-bit input/ output port
P137				SWCLK	
P147		Input/ Output	Analog function	ANI12/VREF0/VCOUT1	Port 14 1-bit input/ output port, can be specified as input or output. The input port can be set by software using internal pull-up resistors. The P147 can be set as an analog input.
RESETB	Type 5	Input	—	—	An input dedicated pin for external reset, which must be connected directly or through a resistor to V_{DD} when external reset is not in use.

4.1.2 32pin product pin function description

(1/ 2)

Function name	Port type	Input/ output	After the reset is released	Multplexing features	Function
P00	Type 1	Input/ Output	Analog function	ANI11/TxD1/VCIN10/TI00/TBCLK0/（TAO）/INTP8/CTxD0	Port 0 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The input of P01 can be set to TTL input buffer. The output of P00 can be set to an N-channel open-drain output (V_{DD} withstand voltage). P00 and P01 can be set as analog inputs.
P01				ANI10/RxD1/VCIN11/TO00/ TBCLK1 /TAIO/INTP10/CRxD0	
P10		Input/ Output	Analog function	SCLK11/SCL11/TMIOB1/ANI9/（TxD2）	Port 1 8-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The inputs of P10 and P14~P17 can be set to TTL Input buffering. The outputs of P10, P11, P13~ P15 and P17 can be set to N-channel open-drain output (V_{DD} withstand voltage). P10 and P11 can be set as analog inputs.
P11				（RxD0）/SDI11/SDA11/TMIOD1/（TMIOA1）/ANI8	
P12			Input port	（TxD0）/SDO11/TMIOA1/（TMIOB0）	
P13				TxD2/SDO20/TMIOC1/（TMIOD1）/IrTxD	
P14				RxD2/SDI20/SDA20/ TMIOB0/（TMIOC1）/（SCLA0）/IrRxD	
P15				SCLK20/SCL20/TMIOD0/（SDAA0）/CLKBUZ1	
P16				TI01/TO01/INTP5/TMIOC0/（RxD0）/（TMIOA1）	
P17				TI02/TO02/TMIOA0/TMCLK/（TxD0）/（TMIOD0）	
P20		Input/ Output	Analog function	ANI0/AVREFP/VCIN12/（INTP11）	Port 2 4-bit input/ output ports that can be specified as inputs or outputs in bits. Can be set as an analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P30		Input/ Output	Input port	INTP3/SCLK00/SCL00/TAO/（TMIOB1）	Port 3 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The inputs of P30 and P31 can be set to TTL input buffering. The outputs of P30 and P31 can be set to N-channel open-drain output (V_{DD} withstand voltage).
P31				TI03/TO03/INTP4/CLKBUZ0/（TAIO）/VCOUT1 /SS00/SCLA0	
P40		Input/ Output	Input port	SWDIO	Port 4 1-bit input/ output port, can be specified as input or output. The input port can be set by software using internal pull-up resistors.

(2/2)

Function name	Port type	Input/ Output	After the reset is released	Multplexing features	Function
P50	Type 1	Input/ Output	Input port	INTP1/SDI00/RxD0/SDA00 /TBIO0/（TAO）/（TMIOC1）/（CRxD0）	Port 5 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The input of the P50 can be set to TTL input buffer. The outputs of the P50 and P51 can be set to an open-drain output of the N-channel (V_{DD} withstand voltage).
P51				INTP2/SDO00/TxD0/TBIO1 /（TMIOD1）/（CTxD0）	
P70	Type 1	Input/ Output	Input port	INTP6/（VCOUT1）	Port 7 4-bit input/output port, which can be specified as input or output in bits. The input port can use internal pull-up resistance through software settings. The input of the P74 can be set to TTL input buffer and the output can be set to an N-channel open-drain output (V_{DD} withstand voltage).
P72				INTP7/（TxD1）	
P73				（RxD1）/（VCOUT0）	
P74				SDAA0	
P120		Input/ Output	Analog function	ANI14/VCOUT0	Port 12 1-bit input/ output port and 2-bit input dedicated port Only the P120 has an output function. Only the input port of the P120 can be set by software to use internal pull-up resistors. The P120 can be set as an analog input.
P121	Type 3	Input	Input port	X1	
P122				X2/EXCLK	
P136	Type 1	Input/ Output	Input port	INTP0	Port 13 2-bit input/ output port
P137				SWCLK	
P147		Input/ Output	Analog function	ANI12/VREF0	Port 14 1-bit input/ output port, can be specified as input or output. The input port can be set by software using internal pull-up resistors. The P147 can be set as an analog input.
RESETB	Type 5	Input	—	—	An input dedicated pin for external reset, which must be connected directly or through a resistor to V_{DD} when external reset is not in use.

Note:

1. Each pin can be set to digital or analog (can be set in bits) via port mode control register x (PMCx).
2. For a description of the multiplexing function, see "4.2 Port Multiplexing Function".
3. The functions in the table above ( ) can be assigned by setting the peripheral I/ O redirection registers.

4.1.3 40pin Product Pin Function Description

(1/2)

Feature name	Port type	Input/ output	After the reset is released	Multplexing features	Function
P00	Type 1	Input/ Output	Analog function	ANI11/TxD1/VCIN10/TI00/TBCLK0 /（TAO）/INTP8/CTxD0	Port 0 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The input of P01 can be set to TTL input buffer. The output of the P00 can be set to an N-channel open-drain output (V_{DD} withstand voltage). P00 and P01 can be set as analog inputs.
P01				ANI10/RxD1/VCIN11/TO00/TBCLK1 /TAIO/INTP10/CRxD0	
P10		Input/ Output	Analog function	SCLK11/SCL11/TMIOB1/ANI9/（TxD2）	Port 1 8-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The inputs of P10 and P14~P17 can be set to TTL input buffer. The outputs of P10, P11, P13~ P15 and P17 can be set to N-channel open-drain outputs (V_{DD} withstand voltage). P10 and P11 can be set as analog inputs.
P11				（RxD0）/SDI11/SDA11/TMIOD1/（TMIOA1）/ANI8	
P12			Input port	（TxD0）/SDO11/TMIOA1/（TMIOB0）	
P13				TxD2/SDO20/TMIOC1/（TMIOD1）/IrTxD	
P14				RxD2/SDI20/SDA20/ TMIOB0/（TMIOC1）/（SCLA0）/IrRxD	
P15				SCLK20/SCL20/TMIOD0/（SDAA0）/CLKBUZ1	
P16				TI01/TO01/INTP5/TMIOC0/（RxD0）/（TMIOA1）	
P17				TI02/TO02/TMIOA0/TMCLK/（TxD0）/（TMIOD0）	
P20		Input/ Output	Analog function	ANI0/AVREFP/VCIN12/（INTP11）	Port 2 6-bit input/ output ports that can be specified as inputs or outputs in bits. Can be set as an analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P24				ANI4/PGA1IN	
P25				ANI5/PGA1GND	
P30		Input/ Output	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO/（TMIOB1）	Port 3 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The input of the P30 can be set to TTL input buffering. The output of the P30 can be set to an N-channel open-drain output (V_{DD} withstand voltage).
P31				TI03/TO03/INTP4/CLKBUZ0/（TAIO）/VCOUT1/SS00	
P40		Input/ Output	Input port	SWDIO	Port 4 1-bit input/ output port, can be specified as input or output. The input port can be set by software using internal pull-up resistors.

(2/ 2)

Function name	Port type	Input/ output	After the reset is released	Multplexing features	function
P50	Type 1	Input/ Output	Input port	INTP1/SDI00/RxD0/SDA00/TBIO0/（TAO）/（TMIOC1）/（CRxD0）	Port 5 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The input of the P50 can be set to TTL input buffer. The outputs of the P50 and P51 can be set to an N-channel open-drain output (V_{DD} withstand voltage).
P51				INTP2/SDO00/TxD0/TBIO1/（TMIOD1）/（CTxD0）	
P60	Type 2	Input/ Output	Input port	SCLA0	Port 6 2-bit input/ output ports that can be specified as inputs or outputs in bits. The output of P60~ P61 is an N-channel open-drain output (6V withstand voltage).
P61				SDAA0	
P70	Type 1	Input/ Output	Input port	KR0/（VCOUT0）/（VCOUT1）	Port 7 5-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The P74 output can be set to an N-channel open-drain output (V_{DD} withstand voltage).
P72				KR2/（TxD1）	
P73				KR3/SDO01/（RxD1）	
P74				KR4/SDI01/SDA01	
P75				KR5/INTP9/SCLK01/SCL01	
P120		Input/ Output	Analog function	ANI14/VCOUT0	Port 12 1-bit input output port and 4-bit input dedicated port Only the P120 has an output function. Only the input port of the P120 can be set by software to use internal pull-up resistors. The P120 can be set as an analog input.
P121	Type 3	Input	Input port	X1	
P122				X2/EXCLK	
P123				XT1	
P124				XT2/EXCLKS	
P136	Type 1	Input/ Output	Input port	INTP0	Port 13 2-bit input/ output port.
P137				SWCLK	
P140		Input/ Output	Input port	CLKBUZ0/INTP6	Port 14 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The P147 can be set as an analog input.
P147			Analog function	ANI12/VREF0	
RESETB	Type 5	Input	—	—	An input dedicated pin for external reset that must be connected to V_{DD} directly or through a resistor when external reset is not in use.

Note:

1. Each pin can be set to digital or analog (can be set in bits) via port mode control register x (PMCx).
2. For a description of the multiplexing function, see "4.2 Port Multiplexing Function".
3. The functions in the table above ( ) can be assigned by setting the peripheral I/ O redirection registers.

4.1.4 48pin Product Pin Function Description

(1/ 2)

Feature name	port type	Input/ output	After the reset is released	Multplexing features	function
P00	Type 1	Input/ Output	Analog function	ANI11/TxD1/VCIN10/TI00/TBCLK0/（TAO）/（INTP8）/CTxD0	Port 0 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The input of P01 can be set to TTL input buffer. The output of the P00 can be set to an N-channel open-drain output (V_{DD} withstand voltage). P00 and P01 can be set as analog inputs.
P01				ANI10/RxD1/VCIN11/TO00/TBCLK1/TAIO/INTP10/CRxD0	
P10		Input/ Output	Analog function	SCLK11/SCL11/TMIOB1/ANI9/（TxD2）	Port 1 8-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The inputs of P10 and P14~P17 can be set to TTL Input buffering. The outputs of P10, P11, P13~P15 and P17 can be set to N-channel open-drain outputs (V_{DD} withstand voltage). P10 and P11 can be set as analog inputs.
P11				（RxD0）/SDI11/SDA11/TMIOD1/（TMIOA1）/ANI8	
P12			Input port	（TxD0）/SDO11/TMIOA1/（TMIOB0）	
P13				TxD2/SDO20/TMIOC1/（TMIOD1）/IrTxD	
P14				RxD2/SDI20/SDA20/ TMIOB0/（TMIOC1）/（SCLA0）/IrRxD	
P15				SCLK20/SCL20/TMIOD0/（SDAA0）/CLKBUZ1	
P16				TI01/TO01/INTP5/TMIOC0/（RxD0）/（TMIOA1）	
P17				TI02/TO02/TMIOA0/TMCLK0/TxD0）/（TMIOD0）	
P20		Input/ Output	Analog function	ANI0/AVREFP/VCIN12/（INTP11）	Port 2 8-bit input/ output ports that can be specified as inputs or outputs in bits. Can be set as an analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P24				ANI4/PGA1IN	
P25				ANI5/PGA1GND	
P26				ANI6	
P27				ANI7	
P30		Input/ Output	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO/（TMIOB1）	Port 3 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The input of the P30 can be set to TTL input buffering. The output of the P30 can be set to an N-channel open-drain output (V_{DD} withstand voltage).
P31				TI03/TO03/INTP4/（CLKBUZ0）/（TAIO）/VCOUT1	
P40		Input/ Output	Input port	SWDIO	Port 4 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors.
P41				（TAIO）	

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Feature name	Port type	Input/ output	After the reset is released	Multplexing features	Function
P50	Type 1	Input/ Output	Input port	INTP1/SDI00/RxD0/SDA00/TBIO0/（TAO）/（TMIOC1）/（CRxD0）	Port 5 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The input of the P50 can be set to TTL input buffer. The outputs of the P50 and P51 can be set to an open-drain N-channel output (V_{DD} withstand voltage).
P51				INTP2/SDO00/TxD0/TBIO1/（TMIOD1）/（CTxD0）	
P60	Type 2	Input/ Output	Input port	SCLA0	Port 6 4-bit input/ output ports that can be specified as inputs or outputs in bits. The output of P60~ P63 is an N-channel open-drain output (6V withstand voltage).
P61				SDAA0	
P62				SS00	
P63				—	
P70	Type 1	Input/ Output	Input port	KR0/SCLK21/SCL21/（VCOUT1）	Port 7 6-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The outputs of the P71 and P74 can be set to an open-drain N-channel output (V_{DD} withstand voltage).
P71				KR1/SDI21/SDA21/（VCOUT0）	
P72				KR2/SDO21/（TxD1）	
P73				KR3/SDO01/（RxD1）	
P74				KR4/INTP8/SDI01/SDA01	
P75				KR5/INTP9/SCLK01/SCL01	
P120		Input/ Output	Analog function	ANI14/VCOUT0	Port 12 1-bit input/ output port and 4-bit input dedicated port. Only the P120 has an output function. Only the input port of the P120 can be set by software to use internal pull-up resistors. The P120 can be set as an analog input.
P121	Type 3	Input	Input port	X1	
P122				X2/EXCLK	
P123				XT1	
P124				XT2/EXCLKS	
P130	Type 4	Output	Output port	—	Port 13 1-bit output dedicated port and 2-bit input/ output port, P137 can be specified as input or output in bits. The input port can be set by software using internal pull-up resistors.
P136	Type 1	Input/ Output	Input port	INTP0	
P137				SWCLK	
P140		Input/ Output	Input port	CLKBUZ0/INTP6	Port 14 3-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. P146, P147 can be set as analog inputs.
P146			Analog function	ANI15	
P147				ANI12/VREF0	
RESETB	Type 5	Input	—	—	Input dedicated pin for external reset When no external reset is used, it must be connected to V_{DD} directly or through a resistor.

Note:

1. Each pin can be set to digital or analog (can be set in bits) via port-mode control register x (PMCx).
2. For a description of the multiplexing function, see "4.2 Port Multiplexing Function".
3. The functions in the table above ( ) can be assigned by setting the peripheral I/ O redirection registers.

4.1.5 64pin Product Pin Function Description

(1/2)

Function name	Port type	Input/ Output	After the reset is released	Multplexing features	Function description
P00	Type 1	Input/ output	Input port	TI00/TBCLK0/（TAO）/（INTP8）	Port 0 7-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The inputs of P01, P03 and P04 can be set to TTL Input buffering. The outputs of P00 and P02~P04 can be set to N-channel open-drain output (EV_{DD} withstand voltage). P02, P03, P04 can be set as analog inputs.
P01				TO00/TBCLK1/TAIO/（INTP10）	
P02			Analog function	ANI11/SDO10/TxD1/VCIN10/CTxD0	
P03				ANI10/SDI10/RxD1/SDA10/VCIN11/CRxD0	
P04				ANI13/SCLK10/SCL10	
P05			Input port	（INTP10）	
P06				（INTP11）/（TAIO）	
P10		Input/ output	Analog function	SCLK11/SCL11/TMIOB1/ANI9	Port 1 8-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The inputs of P10 and P14~P17 can be set to TTL Input buffering. The outputs of P10, P11, P13~P15, and P17 can be set to N-channel open-drain output (EV_{DD} withstand voltage). P10 and P11 can be set as analog inputs.
P11				（RxD0）/SDI11/SDA11/TMIOD1/（TMIOA1）/ANI8	
P12			Input port	（TxD0）/SDO11/TMIOA1/（TMIOB0）/（INTP5）	
P13				TxD2/SDO20/TMIOC1/（TMIOD1）/IrTxD	
P14				RxD2/SDI20/SDA20/TMIOB0/（TMIOC1）/（SCLA0）/IrRxD	
P15				SCLK20/SCL20/TMIOD0/（SDAA0）	
P16				TI01/TO01/INTP5/TMIOC0/（SDI00）/（RxD0）/（TMIOA1）	
P17				TI02/TO02/TMIOA0/TMCLK0/（SDO00）/（TxD0）/（TMIOD0）	
P20		Input/ output	Analog function	ANI0/AVREFP/VCIN12/（INTP11）	Port 2 8-bit input/ output ports that can be specified as inputs or outputs in bits. Can be set as an analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P24				ANI4/PGA1IN	
P25				ANI5/PGA1GND	
P26				ANI6	
P27				ANI7	
P30		Input/ output	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO/（TMIOB1）	Port 3 2-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The input of the P30 can be set to TTL input buffering. The output of the P30 can be set to an N-channel open-drain output (EV_{DD} withstand voltage).
P31				TI03/TO03/INTP4/（CLKBUZ0）/（TAIO）/VCOUT1	

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Function name	Port type	Input/ output	After the reset is released	Multplexing features	Function
P40	Type 1	Input/ Output	Input port	SWDIO	Port 4 4-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors.
P41				（TAIO）	
P42				（INTP8）	
P43				（INTP9）	
P50		Input/ Output	Input port	INTP1/SDI00/RxD0/SDA00/TBIO0/（TAO）/（TMIOC1）/（CRxD0）	Port 5 6-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The inputs of the P50 and P55 can be set to TTL input buffering. The outputs of the P50, P51, and P55 can be set to an N-channel open-drain output (EV_{DD} withstand voltage).
P51				INTP2/SDO00/TxD0/TBIO1/（TMIOD1）/（CTxD0）	
P52				（INTP1）	
P53				（INTP2）	
P54				（INTP3）	
P55				（INTP4）/（CLKBUZ1）/（SCLK00）	
P60	Type 2	Input/ Output	Input port	SCLA0	Port 6 4-bit input/ output ports that can be specified as inputs or outputs in bits. The output of P60~ P63 is an N-channel open-drain output (6V withstand voltage).
P61				SDAA0	
P62				SS00	
P63				—	
P70	Type 1	Input/ Output	Input port	KR0/SCLK21/SCL21/（VCOUT1）	Port 7 8-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. The outputs of the P71 and P74 can be set to an open drain output of the N-channel (EV_{DD} withstand voltage).
P71				KR1/SDI21/SDA21/（VCOUT0）	
P72				KR2/SDO21	
P73				KR3/SDO01	
P74				KR4/INTP8/SDI01/SDA01	
P75				KR5/INTP9/SCLK01/SCL01	
P76				KR6/INTP10/（RxD2）	
P77				KR7/INTP11/（TxD2）	
P120		Input/ output	Analog function	ANI14/VCOUT0	Port 12 1-bit input/ output port and 4-bit input dedicated port, Only P120 can specify inputs or outputs. Only the input port of the P120 can be set by software to use internal pull-up resistors. The P120 can be set as an analog input
P121	Type 3	Input	Input port	X1	
P122				X2/EXCLK	
P123				XT1	
P124				XT2/EXCLKS	
P130	Type 4	Output	Output port	—	Port 13 1-bit output dedicated port and 1-bit input/ output port, P137 can be specified as input or output in bits. The input port can be set by software using internal pull-up resistors.
P136	Type 1	Input/ Output	Input port	INTP0	
P137				SWCLK	
P140		Input/ Output	Input port	CLKBUZ0/INTP6	Port 14 4-bit input/ output ports that can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors. P146, P147 can be set as analog inputs.
P141				CLKBUZ1/INTP7	
P146			Analog function	ANI15	
P147				ANI12/VREF0	
RESETB	Type 5	Input	—	—	An input dedicated pin for external reset that must be connected to V_{DD} directly or by resistor when external reset is not in use.

Note:

1. Each pin can be set to digital or analog (can be set in bits) via port-mode control register x (PMCx).
2. For a description of the multiplexing function, see "4.2 Port Multiplexing Function".
3. The functions in the table above ( ) can be assigned by setting the peripheral I/ O redirection registers.

4.2 Port Multiplexing Feature

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Feature name	Input/Output	Function
ANI0 ~ ANI15	Input	Analog input of the A/D converter
ANO0, ANO1	Output	The output of the D/A converter
INTP0 ~ INTP11	Input	An external interrupt requests input Designation of valid edges: rising edge, falling edge, rising and falling bilateral edges
VCIN0	Input	The analog voltage input of comparator 0
VCIN10, VCIN11, VCIN12 VCIN13	Input	The analog voltage/ reference input of Comparator 1
VREF0	Input	Reference input for comparator 0
VCOUT0, VCOUT1	Output	Comparator output
PGA0IN, PGA1IN	Input	PGA input
PGA0GND, PGA1GND	Input	PGA reference input
KR0 ~ KR7	Input	key to interrupt input
CLKBUZ0, CLKBUZ1	Output	Clock output/ buzzer output
RTC1HZ	Output	Correction clock (1Hz) output of the real-time clock
RESETB	Input	The active-low system reset input must be connected to VDD directly or via a resistor when no external reset is in use.
CRxD0	Input	Serial data input for CAN
CTxD0	Output	Serial data output of CAN
IrRxD	Input	Serial data input for IrDA
IrTxD	Output	Serial data output of IrDA
RxD0 ~ RxD2	Input	Serial interfaces for serial data input for UART0, UART1, UART2
TxD0 ~ TxD2	Output	Serial interface UART0, UART1, UART2 serial data output
SCL00, SCL01, SCL10 SCL11, SCL20, SCL21	Output	Serial interface IIC00, IIC01, IIC10, IIC11, IIC20, IIC21 serial clock output
SDA00, SDA01, SDA10 SDA11, SDA20, SDA21	Input/Output	Serial data input/ output for serial interfaces IIC00, IIC01, IIC10, IIC11, IIC20, IIC21
SCLK00, SCLK01 SCLK10, SCLK11 SCLK20, SCLK21	Input/Output	Serial interfaces SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21 Serial clock input/ output
SDI00, SDI01, SDI10 SDI11, SDI20, SDI21	Input	Serial interfaces SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21 serial data input

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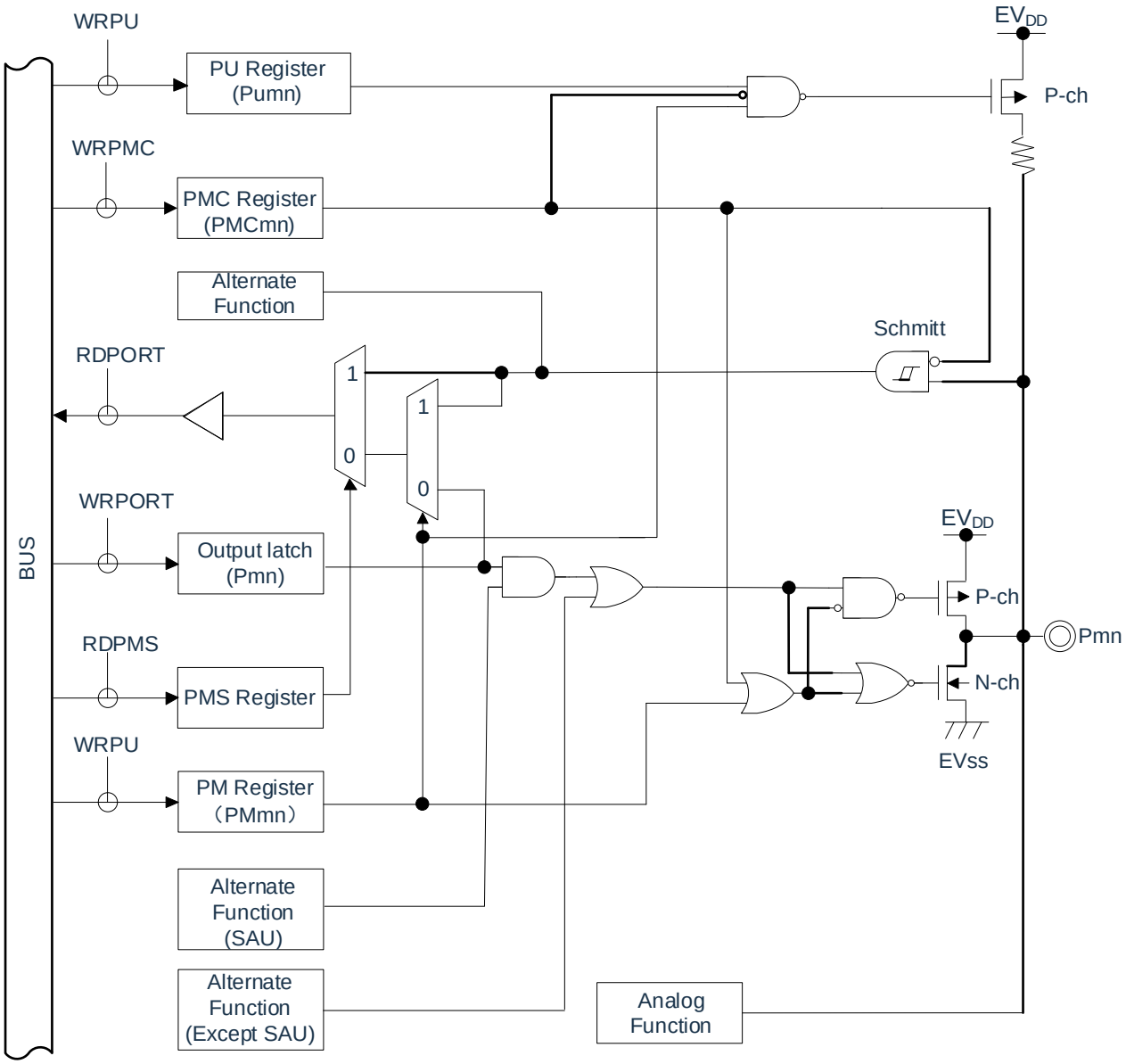
Feature name	Input/Output	Function
SS00	Input	Serial interface SSPI00 chip select input
SDO00,SDO01,SDO10 SDO11,SDO20,SDO21	Output	Serial data output for SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21
SCLA0	Input/Output	Serial interface IICA0 clock input/ output
SDAA0	Input/Output	Serial interface Serial data input/ output of IICA0
TI00~ TI03	Input	External counting clock/ capture trigger input of the 16-bit timer Timer4
TO00~ TO03	Output	The timer output of the 16-bit timer Timer4
TAIO	Input/Output	The input/ output of the timer TimerA
MAN	Output	The output of the timer TimerA
TMCLK	Input	External clock input for the timer TimerM
TMIOA0, TMIOB0, TMIOC0 TMIOD0, TMIOA1, TMIOB1 TMIOC1, TMIOD1	Input/Output	Input/ output of the timer TimerM
TBIO0, TBIO1	Input/Output	The input/ output of the timer TimerB
TBCLK0, TBCLK1	Input	External clock input for the timer TimerB
X1, X2	—	Connect the resonator used for the main system clock.
EXCLK	Input	External clock input for the main system clock
XT1, XT2	—	Connect the resonator used for the secondary system clock.
EXCLKS	Input	External clock input for the secondary system clock
V_{DD}	—	＜24Pins,32Pins,40Pins,48Pin product＞:Power supply for all pins ＜64Pin product＞: Power supplies for P20~P27, P121~P124, P137 and RESETB pins
EV_{DD}	—	Power supply for port pins (except P20~P27, P121~P124, P137, and RESETB).
AV_{REFP}	Input	The positive (+) reference input of the A/ D converter
AV_{REFM}	Input	The negative (-) reference input of the A/ D converter
V_{SS}	—	＜24Pins,32Pins,40Pins,48Pin product＞: Ground potential of all pins ＜64Pin product＞: Ground potential of P20~P27, P121~P124, P137 and RESETB pins
EV_{SS}	—	The ground potential of the port pins (except P20~P27, P121~P124, P137, and RESETB).
SWDIO	Input/Output	SWD data interface
SWCLK	Input	SWD clock interface

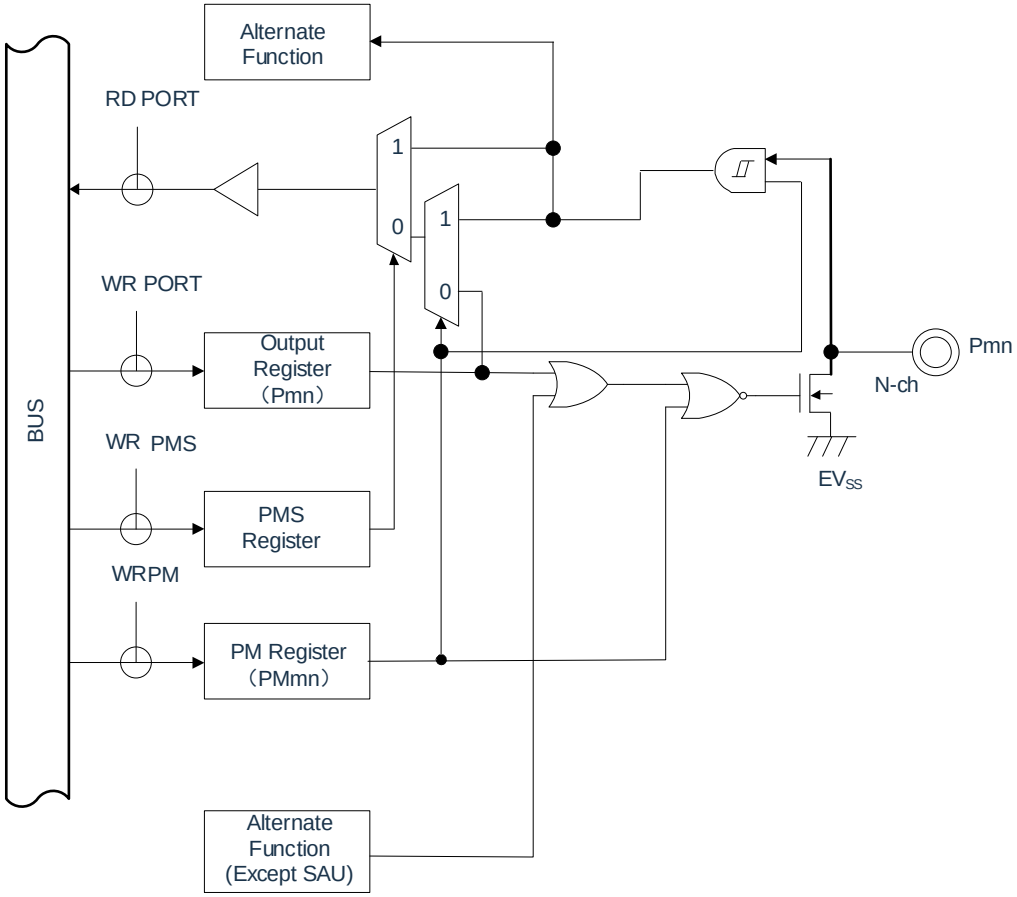
Note: As a countermeasure against noise and lockout, the bypass capacitor (about 0.1uF) must be connected with the shortest distance between V_{DD}-V_{SS} and EV_{DD}-EV_{SS} and with thick wiring.

4.3 Port Type

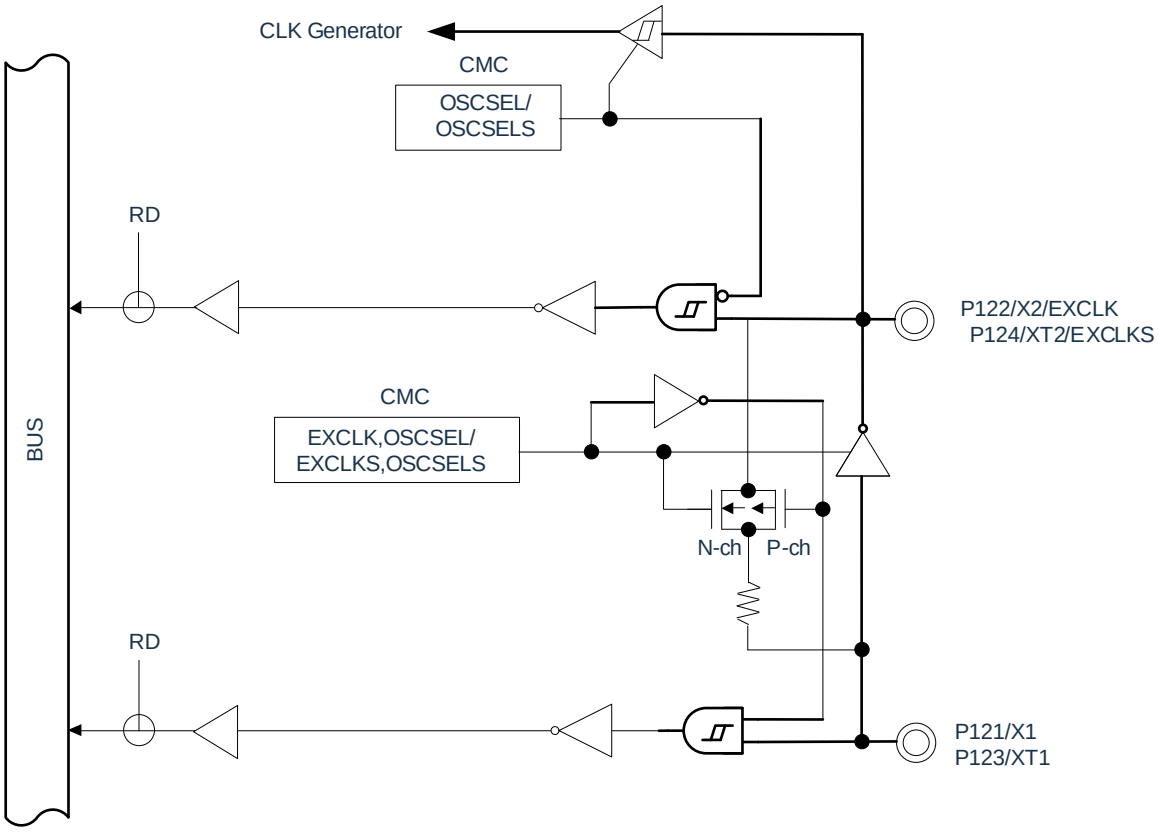
Type 1: Bidirectional I/ O capability



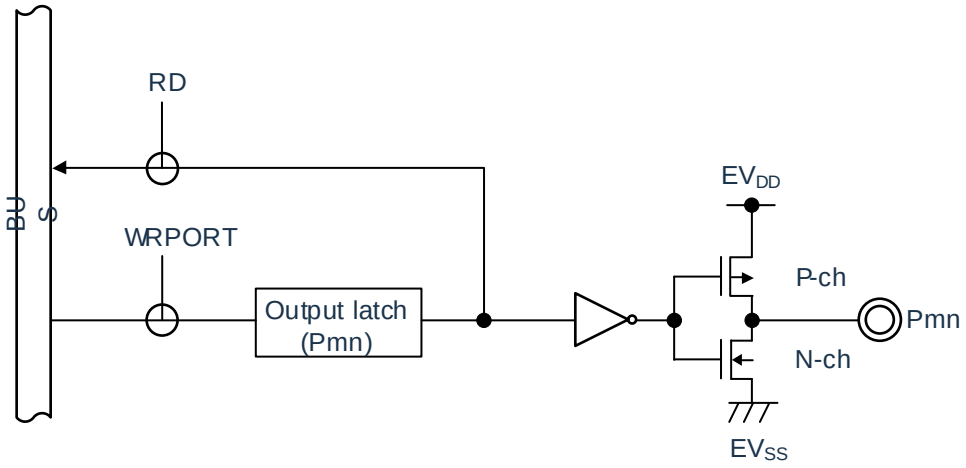
Type 2: NOD function



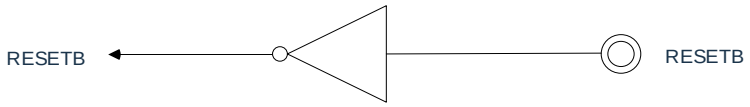
Type 3: Input function only



Type 4: Output function only



Type 5: RESET function



5 Functional Summary

5.1 ARM® Cortex-M0®+ Core

ARM's Cortex-M0+ processor is the next generation of ARM processors for embedded systems. It provides a low-cost platform designed to meet the needs of low-pin-count and low-power microcontrollers while providing excellent computing performance and advanced system response to interrupts.

The Cortex-M0+ processor's 32-bit RISC processor provides superior code efficiency and delivers the high performance expectations of an ARM core, unlike 8-bit and 16-bit devices of the same memory size. The Cortex-M0+ processor has 32 address lines and up to 4G of storage.

The Cortex-M0+ processor equipped with this product integrates an MPU memory protection unit: it provides hardware management and protection of memory and control access rights.

The BAT32A237 uses an embedded ARM core, making it compatible with all ARM tools and software.

5.2 Memory

5.2.1 Flash Memory

The BAT32A237 has built-in flash memory that can be programmed, erased, and rewritten. It has the following functions:

- Programs and data sharing 128K storage.
- 1.5KB dedicated data Flash memory.
- Support page erasure, the size of each page is 512byte.
- Supports byte/ half-word/ word (32bit) programming.

5.2.2 SRAM

The BAT32A237 contains 12KB of embedded SRAM.

5.3 Enhanced DMA Controller

Built-in Enhanced DMA (Direct Memory Access) controller enables data transfer between memories without using a CPU.

- DMA can be started via peripheral function interrupts, enabling real-time control through communication, timers, and A/ D.
- The transmission source/ destination field is optional for the full address space range (when the flash field is used as the destination address, flash needs to be preset as the programming mode).
- Supports 4 modes (normal transfer mode, repeated transfer mode, block transfer mode and chain transfer mode).

5.4 Linkage Controller

The linkage controller links the events output by each peripheral function with the peripheral function trigger source. This enables collaborative operation between peripheral functions without using a CPU.

The linkage controller has the following functions:

- It can link event signals together to realize the linkage of peripheral functions.
- There are 22 types of event input and 10 types of event triggering.

5.5 The Clock Generation and Start Up

A clock generation circuit is a circuit that generates a clock to the CPU and peripheral hardware. There are three types of system clocks and clock oscillation circuits.

5.5.1 Master System Clock

- X1 oscillation circuit: can generate 1~20MHz clock oscillation by connecting the resonator to the pins (X1 and X2), and can perform deep sleep Command or set MSTOP to stop oscillation.
- High-speed internal oscillator (high-speed OCO): Oscillation can be performed by selecting the frequency by the option byte. After unreset, the CPU starts running at this high-speed internal oscillator clock by default. Oscillation can be stopped by executing a deep sleep command or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed internal oscillator. The maximum frequency is 64MHz with an accuracy ± 1.0%.
- Input external clock from pin (X2): (1~20MHz), and the input of the external main system clock can be invalidated by executing the deep sleep command or setting the MSTOP bit.

5.5.2 Secondary System Clock

- XT1 oscillation circuit: Generates a clock oscillation of 32.768 KHz by connecting a 32.768KHz resonator to the pins (XT1 and XT2) and can be set The XTSTOP bit stops the oscillation.
- Input of the external clock from pin (XT2): 32.768KHz, and the input of the external clock can be invalidated by setting the XTSTOP bit.

5.5.3 Low Speed Internal Oscillator Clock

Low-speed internal oscillator (low-speed OCO): Generates 15KHz (typical) clock oscillation. You cannot use a low-speed internal oscillator clock as a CPU clock. Only the following peripheral hardware can operate through the low-speed internal oscillator clock:

- Watchdog Timer (WWDT)
- Real-Time Clock (RTC)
- 15-bit interval timer
- Timer TimerA

5.6 Power Management

5.6.1 Power Supply Mode

V_{DD}: External power supply with a voltage range of 2.0 to 5.5V.

EV_{DD}: External power supply with voltage range of 2.0 to 5.5V.

The voltage of the V_{DD} pin must be equal to the voltage of the EV_{DD} pin.

5.6.2 Power-on Reset

The power-on reset circuit (POR) has the following functions.

- An internal reset signal is generated when power is applied. If the supply voltage (V_{DD}) is greater than the sense voltage (V_{PER}), the reset is released. However, the reset state must be maintained by a voltage detection circuit or an external reset until the operating voltage range is reached.
- Set the supply voltage (V_{DD}) and the detection voltage (V_{PDR}) to compare, when $V_{DD}<V_{PDR}$, an internal reset signal is generated. However, when the power supply drops, it must be transferred to before it is less than the operating voltage range Deep sleepmode, or set to reset state via voltage detection circuit or external reset. If you want to restart operation, you must confirm that the supply voltage has returned to the operating voltage range.

5.6.3 Voltage Detection

The voltage detection circuit sets the operating mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) via option bytes. The voltage detection (LVD) circuit has the following functions:

- The supply voltage (V_{DD}) and the sense voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) are compared to generate an internal reset or interrupt request signal.
- The sense voltage of the supply voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected by the option byte.
- Can run in deep sleep mode.
- When the power supply rises, it must be maintained in the reset state by voltage detection circuitry or an external reset before reaching the operating voltage range. When the power supply drops, it must be switched to deep sleep mode before it is less than the operating voltage range, or set to reset by voltage detection circuit or external reset.
- The operating voltage range varies depending on the setting of the user option byte.

5.7 Low Power Mode

The BAT32A237 supports two low-power modes to achieve the best compromise between low power consumption, short start-up time, and available wake-up sources

- Sleep mode: Enter sleep mode by executing a sleep instruction. Sleep mode is the mode that stops the CPU from running the clock. Before setting the sleep mode, if the high-speed system clock oscillation circuit, high-speed internal oscillator, or subsystem clock oscillator circuit is oscillating, each clock continues to oscillate. Although this mode does not reduce the operating current to the point of deep sleep mode, it is an effective mode when you want to restart processing immediately with an interrupt request or when you want to run intermittently frequently.
- Deep sleep mode: Enter deep sleep mode by executing deep sleep instructions. Deep sleep mode is a mode that stops the oscillation of the high-speed system clock oscillation circuit and the high-speed internal oscillator and stops the entire system. It can greatly reduce the operating current of the chip. Because deep sleep mode can be dismissed by interrupt requests, intermittent operation is also possible. However, in the case of the X1 clock, because it is necessary to ensure the waiting time for oscillation stability when the deep sleep mode is removed, the sleep mode must be selected if you must start processing immediately by interrupting the request.

In either mode, the registers, flags, and data memory are all kept as they were before standby mode, and the output latches and output buffers of the input/ output ports are also maintained.

5.8 Reset Function

The following seven methods generate a reset signal.

1) An external reset is input via the RESETB pin.
2) An internal reset is generated by program runaway detection by the watchdog timer.
3) An internal reset is generated by comparing the supply voltage and the sense voltage of the power-on reset (POR) circuit.
4) An internal reset is generated by comparing the supply voltage and the sense voltage of the voltage detection circuit (LVD).
5) An internal reset occurs due to a RAM parity error.
6) An internal reset occurred due to access to illegal memory.
7) Software reset

The internal reset is the same as the external reset, and after the reset signal is generated, the procedure is executed from the addresses written in addresses 0000H and 0001H.

5.9 Interrupt Function

The Cortex-M0+ processor has a built-in Nested Vector Interrupt Controller (NVIC) that supports up to 32 interrupt request (IRQ) inputs and one non-maskable interrupt (NMI) input, plus multiple internal exceptions.

This product expands 32 maskable interrupt requests (IRQ) and 1 non-maskable interrupt (NMI) to support up to 64 maskable interrupt sources and one non-maskable interrupt source. The actual number of interrupt sources varies by product.

		24pins	32pins	40pins	48pins	64pins
Interrupts can be masked	external	9	11	11	11	12
	internal	29	29	29	29	29

5.10 Real-time Clock (RTC)

The real-time clock (RTC) has the following functions.

- Counters with years, months, weeks, days, hours, minutes, and seconds.
- Fixed period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month).
- Alarm interrupt function (alarm: week, hour, minute)
- 1Hz pin-out function
- Support the division of the secondary system clock or the main system clock as the operating clock of the RTC
- The real-time clock interrupt signal (INTRTC) can be used as a wake-up for deep sleep mode
- Supports a wide range of clock correction functions

Year, month, week, day, hour, minute, and second counts can only be performed if the secondary system clock (32.768KHz) or the division of the main system clock is selected as the operating clock of the RTC. When a low-speed internal oscillator clock (15KHz) is selected, only the fixed-period interrupt function can be used.

5.11 Watchdog Timer

1-channel WWDT, 17bit watchdog timer runs with option byte set count. The watchdog timer operates on a low-speed internal oscillator clock (15KHz). Watchdog timers are used to detect program runaways. When a program runaway is detected, an internal reset signal is generated.

The following are judged to be out of control:

- When the watchdog timer counter overflows
- When a 1-bit operation instruction is executed on the watchdog timer allowable register (WDTE).
- When writing data other than "ACH" to WDTE registers
- When writing data to WDTE registers during window closure

5.12 SysTick Timer

This timer is exclusive to real-time operating systems, but can also be used as a standard decrement counter.

It features a 24-bit decrement counter when the self-loading capacity counter reaches 0, and a maskable system interrupt is generated.

5.13 Timer4

This product has a built-in timer unit Timer4 containing four 16-bit timers. Each 16-bit timer is called a "channel" and can be used as a stand-alone timer or combined with multiple channels for advanced timer functions.

Please refer to the table below for details on each function.

Independent channel operation function	Multi-channel linkage operation function
● Interval timer ● Square wave output ● External event counters ● Frequency divider ● Input pulse interval measurement ● Measurement of the high/ low width of the input signal ● Latency counter	● Single trigger pulse output ● PWM output ● Multiple PWM outputs

5.13.1 Independent Channel Operation Function

The independent channel operation function is the ability to use any channel independently of other channel operating modes. The independent channel operation feature is used as the following mode:

1) Interval Timer: Can be used as a reference timer for generating interrupts at fixed intervals (INTTM).
2) Square wave output: Whenever an INTTM interrupt is generated, a flip is triggered to output a 50% duty cycle square wave from the timer output pin (TO).
3) External Event Counter: Counts the effective edge of the input signal of the timer input pin (TI) and can be used as an event counter to generate an interrupt if the specified number of times is reached.
4) Divider function (limited to channel 0 of unit 0): divides the input clock of the timer input pin (TI00) and outputs it from the output pin (TO00).
5) Measurement of input pulse interval: The interval between input pulses is measured by starting counting at the effective edge of the input pulse signal at the timer input pin (TI) and capturing the count value at the effective edge of the next pulse.
6) High/ low width measurement of input signal: Measure the high or low width of the input signal by starting counting on one edge of the input signal of the timer input pin (TI) and capturing the count value on the other edge.
7) Delay Counter: Starts counting at the effective edge of the input signal at the timer input pin (TI) and generates an interrupt after an arbitrary delay period has elapsed.

5.13.2 Multi-channel Linkage Operation Function

The multi-channel linkage operation function is a function that combines the master channel (the reference timer for the main control period) and the slave channel (the timer that follows the operation of the master channel). The multi-channel linkage function can be used in the following modes:

1) Single trigger pulse output: Two channels are used in pairs to generate a single trigger pulse that can arbitrarily set the output timing and pulse width.
2) PWM (Pulse Width Modulation) output: Two channels are used in pairs to generate pulses that can set the period and duty cycle arbitrarily.
3) Multiple PWM (Pulse Width Modulation) outputs: Up to 3 PWM signals with arbitrary duty cycles can be generated at a fixed period by expanding the PWM function and using one master channel and multiple slave channels.

5.13.3 8-bit Timer Operation Function

The 8-bit timer run function uses the 16-bit timer channel as the function of two 8-bit timer channels. (Only Channel 1 and Channel 3 can be used).

5.13.4 LIN-bus Support Features

The Timer4 unit can be used to check whether the received signal in the LIN-bus communication is suitable for the LIN-bus communication format.

1) Wake-up signal detection: The low-level width is measured by starting counting on the falling edge of the input signal on the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the low width is greater than or equal to a fixed value, it is considered a wake-up signal.
2) Detection of the spaced field: After a wake-up signal is detected, the low-level width is measured by starting counting from the falling edge of the input signal of the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the width of the low level is greater than or equal to a fixed value, it is considered to be a spaced field.
3) Measurement of synchronous field pulse width: After detecting the spaced field, measure the low and high level widths of the input signal of the UART serial data input pin (RxD). Based on the bit spacing of the synchronous field measured in this way, the baud rate is calculated.

5.14 TimerA

This product has a built-in 16bit timer TimerA, consisting of a reload register and a decrement counter. Available for the following operating modes:

- Timer mode: Counts the counting source (the counting source can be a clock or an external event)
- Pulse output mode: Counts the counting source and outputs a pulse when overflowing
- Event Counting Mode: Counts external events and works in deep sleep mode.
- Pulse width measurement mode: Measurement of external pulse width
- Pulse period measurement mode: Measurement of external pulse period

5.15 TimerM

This product has a built-in 2-channel 16bit timer TimerM optimized for motor control, which has the following 4 operating modes:

- Timer mode:
  - Input capture function (external signal as trigger, count value to register)
  - Output comparison function (detects whether the count value and register value are the same, and can change the output of the pin during detection)
  - PWM function (continuous output of arbitrary pulse width)
- Reset synchronous PWM mode: output sawtooth wave modulated, dead time-free three-phase waveform (6 pcs)
- Complementary PWM mode: output triangle wave modulation, three-phase waveform with dead time (6 pcs)
- PWM3 mode: output the same period PWM waveform (2 pcs)

5.16 TimerB

This product has a built-in 16-bit timer TimerB, which has the following 3 modes:

- Timer mode:
  - Input snapping function counts on both sides of the rising edge, falling edge, or rising/ falling edge.
  - Output comparison function "L" level output, "H" level output or alternating output
- PWM mode: PWM output capable of arbitrary duty cycle.
- Phase counting mode: The counting value of the 2-phase encoder can be measured automatically.

5.17 TimerC

This product includes a 16-bit timer TimerC that can be triggered by software, comparator, or timer TimerM for input capture.

5.18 15-bit Interval Timer

This product has a built-in 15-bit interval timer that generates interrupts (INTIT) at pre-set intervals and can be used to wake up from deep sleep mode.

5.19 Clock Output/Buzzer Output Control Circuit

The clock output controller is used to provide the clock to the peripheral IC, and the buzzer output controller is used to output the square wave of the buzzer frequency. A dedicated pin provides either a clock output or a buzzer output.

5.20 Universal Serial Communication Unit

This product has built-in 2 universal serial communication units, each unit has a maximum of 4 serial communication channels. It can implement standard SPI, simple SPI, UART and simple I^2C communication functions. Taking the 64pin product as an example, the function distribution of each channel is as follows:

5.20.1 3-wire Serial Interface (Simple SPI)

Data is sent and received synchronously with the serial clock (SCK) output of the master device.

This is using 1 serial clock (SCK), 1 transmit serial data (SO), and 1 receive serial data (SI) for a total of 3 A clock synchronization communication interface for communication lines.

[Sending and receiving of data].

- 7 or 8 bits of data length
- Phase control of transmitted and received data
- MSB/ LSB preferred

[Clock Control].

- Master or subordinate choice
- Phase control of input/ output clocks
- Transmission cycles generated by prescalers and channel internal counters
- Maximum transfer rate

  Master communication: Max. F_{CLK}/ 2

  Dependent communication: Max. F_{MCK}/ 6

[Interrupt function].

- End-of-transfer interrupt, buffer null interrupt

[Error Detection Flag].

- Overflow error

5.20.2 SPI With Slave Chip Selection

SPI serial communication interface that supports slave chip select inputs. This is done using one slave chip select input (SSI), one serial clock (SCK), one transmit serial data (SO), and one receive serial data (SI). Clock synchronization communication interface for communication between 4 communication lines.

[Sending and receiving of data].

- 7 or 8 bits of data length
- Phase control of transmitted and received data
- MSB/ LSB preferred
- Level setting for transmitted and received data

[Clock Control].

- Phase control of input/ output clocks
- Transmission cycles generated by prescalers and channel internal counters
- Maximum transfer rate

  Dependent Communications: Max. F_{MCK}/ 6

[Interrupt function].

- End-of-transfer interrupt, buffer null interrupt

[Error Detection Flag].

- Overflow error

5.20.3 UART

This function enables asynchronous communication over two lines, serial data transmission (TxD) and serial data reception (RxD). Using these two communication lines, data is sent and received asynchronously (using internal baud rates) with other communicating parties in the data frame (consisting of start bits, data, parity bits, and stop bits). Full-duplex UART communication can be implemented by using two channels, dedicated to transmit (even channels) and dedicated to receiving (odd channels), and LIN-bus can also be supported by combining a Timer4 unit and an external interrupt (INTP0).

[Sending and receiving of data].

- Data length of 7, 8, or 9 bits
- MSB/ LSB preferred
- Level setting and inverting selection of transmitted and received data
- Additional, parity function of the parity bit
- Additional stop bits, detection of stop bits

[Interrupt function].

- End-of-transfer interrupt, buffer null interrupt
- Error interrupts caused by frame errors, parity errors, or overflow errors

[Error Detection Flag].

- Frame errors, parity errors, overflow errors

[LIN-bus function].

- Detection of wake-up signals
- Detection of spaced fields (BF).
- Measurement of synchronous fields, calculation of baud rate

5.20.4 Simple I²C

This function enables clock synchronization communication with multiple devices via two lines, serial clock (SCL) and serial data (SDA). Because this simple I²C is designed for single communication with devices such as flash memory and A/ D converters, it can only be used as a master control device. Start and stop conditions, like the operation control registers, must comply with the AC characteristics and are handled by software.

[Sending and receiving of data].

- Master send, master receive (limited to single master master function)
- ACK output function, ACK detection function
- 8-bit data length (when sending the address, specify the address with the highest 7 bits, and use the lowest bit for R/ W control).
- Start and stop conditions are generated by software

[Interrupt function].

- The transfer ended interrupted

[Error Detection Flag].

- ACK error, overflow error

[Simple I²C unsupported features].

- Slave send, slave receive
- Multi-master function (arbitration failure detection function)
- Wait for the detection function

5.21 Standard Serial Interface IICA

The serial interface IICA has the following 3 modes:

- Run-stop mode: This is the mode used when serial transmission is not taking place to reduce power consumption.
- I^2C bus mode (supports multi-master): This mode transmits 8-bit data to multiple devices over 2 wires of a serial clock (SCLA) and a serial data bus (SDAA). Compliant with the I^2C bus format, the master device can generate "start condition", "address", " Indication of transfer direction", "Data" and "Stop condition" . The Satellite automatically detects the received status and data through hardware. This feature simplifies the I^2C bus control portion of the application. Because the SCLA pin and SDAA pin of the serial interface IICA are used as open-drain outputs, pull-up resistors are required for the serial clock line and serial data bus.
- Wake mode: In deep sleep mode, when an extension code or local station address is received from the master device, the deep sleep mode can be lifted by generating an interrupt request signal (INTIICA). This is set via the IICA control register.

5.22 Controller CAN

Universal CAN controller interface function in accordance with the CAN protocol in accordance with the standard in ISO 11898.

- Complies with ISO 11898 and is tested according to ISO/ DIS 16845 (CAN compliance).
- Standard and extended frames are used for receive and transmit
- Communication speed: up to 1Mbps. (CAN input clock greater than or equal to 8MHz)
- 16 message buffers for 1 channel
- Receive/ send history list function
- Automatic block transfer function
- Multi-cache receive block function
- Masking settings for four modes per channel

5.23 Analog-to-digital Converters (ADC)

This product has a built-in 12-bit resolution analog-to-digital converter SARADC, which can convert analog inputs to digital values, and supports up to 16 channels of ADC analog inputs (ANI0~ANI15). The ADC includes the following features:

- 12-bit resolution, slew rate1.06Msps.
- Triggering mode: support software triggering, hardware triggering and hardware triggering in standby state
- Channel selection: Supports both single-channel selection and multi-channel scanning
- Conversion mode: supports single conversion and continuous conversion
- Operating voltage: Supports 2.0V≤V_{DD}≤5.5V operating voltage range
- It can detect the built-in reference voltage (1.45V) and temperature sensors.

The ADC can set various A/ D conversion modes using the following mode combinations.

Trigger mode	Software triggered	Start the conversion through software operations.
	Hardware-triggered no-wait mode	Start the conversion by detecting the hardware trigger.
	The hardware triggers the wait mode	In the transition standby state when the power is cut off, the power is switched on by detecting a hardware trigger, and the conversion automatically starts after the A/ D power supply stabilization waiting time has passed.
Channel selection mode	Select a mode	Select 1 channel of analog input for A/ D conversion.
	Scan mode	A/ D convert the analog inputs of the four channels sequentially. ANI0~ ANI15 can be selected as analog inputs for 4 consecutive channels.
Conversion mode	Single conversion mode	Perform 1 A/ D conversion on the selected channel.
	Continuous conversion mode	Continuous A/ D conversion of the selected channel until stopped by the software.
Sample time/ conversion time	Number of sample clocks/ conversion clocks	The sample time can be set by registers, and the default value for the number of sample clocks is 13.5 clk, and the conversion clock number minimum value is 31.5 clks.

5.24 Digital-to-analog Converters (DAC)

This product has a built-in 2-channel 8-bit resolution analog-to-digital converter DAC that converts the digital input to an analog signal. Has the following characteristics:

- 8-bit resolution D/ A converter
- Supports the output of two independent analog channels
- R-2R ladder network
- Built-in real-time output

5.25 Programmable Gain Amplifier (PGA)

This product has two built-in programmable gain amplifiers (PGA0 and PGA1) with the following functions:

- There are 7 options for amplification gain per PGA: 4x, 8x, 10x, 12x, 14x, 16x, 32x
- An external pin can be selected as ground for the negative feedback resistor of the PGA .
- The output of PGA0 can be selected as an analog input for the A/ D converter or an analog input at the positive side of Comparator 0 (CMP0).
- The output of PGA1 can be selected as an analog input for the A/ D converter

5.26 Comparator (CMP)

This product has built-in two-channel comparators CMP0 and CMP1 with the following features:

- CMP1 external input and reference multi-channel optional.
- The external reference input and internal reference voltage can be selected for the reference voltage.
- The cancellation width of the noise cancellation digital filter can be selected.
- It can detect the active edge of the comparator output and generate an interrupt signal.
- It can detect the active edge of the comparator output and output the event signal to the linkage controller.

5.27 Two-wire Serial Debug Port (SW-DP)

ARM's SW-DP interface allows connection to microcontrollers via serial wire debug tools.

5.28 Security Features

5.28.1 Flash CRC Computing Function (High-speed CRC, General-purpose CRC)

Data errors in flash memory are detected by CRC operations.

The following two CRCs can be used according to different applications and usage conditions.

- High-speed CRC: During the initialization program, it can stop the CPU and check the entire code flash area at high speed.
- General purpose CRC: In CPU operation, it is not limited to the code flash memory area but can be used for multi-purpose inspection.

5.28.2 RAM Parity Error Detection

When reading RAM data, detect parity errors.

5.28.3 SFR Protection Features

Prevent the rewriting of important SFRs (Special Function Registers) due to CPU runaways.

5.28.4 Illegal Memory Access Detection Function

Detects illegal access to areas of illegal memory (areas with no memory or areas with restricted access).

5.28.5 Frequency Detection Function

The Timer4 unit can be used to self-detect the CPU or peripheral hardware clock frequency.

5.28.6 A/D Testing Capabilities

A/ D is performed by A/ D converting the positive (+) reference, negative (-) reference, analog input channel (ANI), temperature sensor output voltage, and internal reference voltage of the A/ D converter The converter performs a self-test.

5.28.7 Digital Output Signal Level Detection Function at Input/ output Ports

When the input/ output port is in output mode, the output level of the pin can be read.

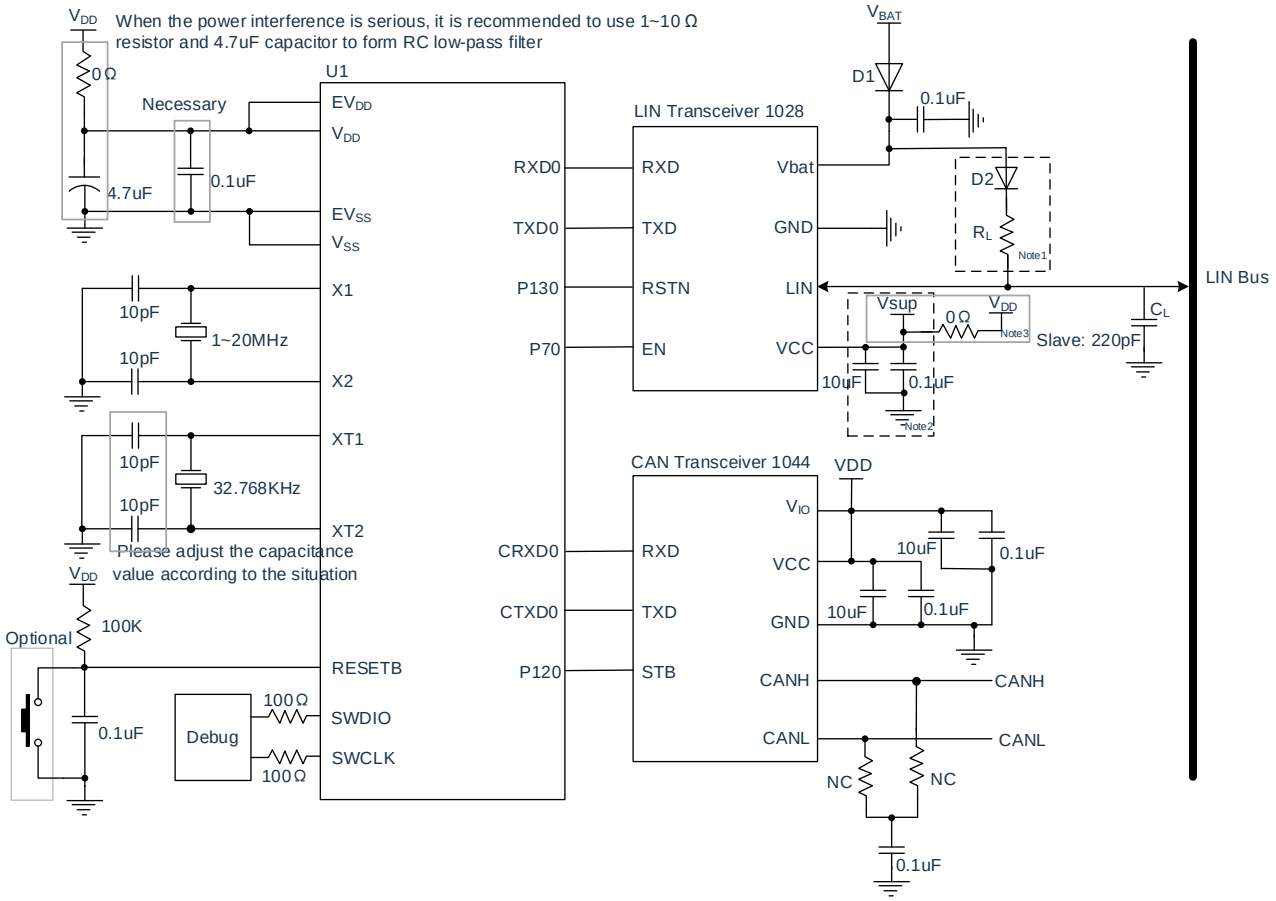
5.29 Key Function

The falling edge can be input through the key interrupt input pin (KR0~KR7) to generate a key interrupt (INTKR).

6 Electrical Characteristics

6.1 Typical Application Peripheral Circuits

The device connection reference for peripheral circuits typical MCU applications is as follows:



Note 1: D2 should be connected only when it is used as a host node, and a 660Ω/6.8nF RL/CL combination is recommended when the RL is used as a host node to obtain a slower slope of the bus waveform;

Note 2: The LIN transceiver 1028 has an internal LDO that can provide a 5V power supply for the system through the VCC pin.

Note 3: Vsup is the 5V power supply output from the 1028, while VDD is the system power supply.

6.2 Absolute Maximum Voltage Rating

(T_A= -40~125°C)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		-0.5~+6.5	V
	EV_{DD}		-0.5~+6.5	V
Input voltage	V_{I1}	P00~P06, P10~P17, P30, P31, P40~P43, P50~P55 P70~P77, P120, P136, P140, P141, P146, P147	-0.3~EV_{DD}+0.3 and -0.3~V_{DD}+0.3 Note 1	V
	V_{I2}	P60~P63(N-channel open drain)	-0.3~+6.5	V
	V_{I3}	P20~P27, P121~P124, P137, EXCLK, EXCLKS RESETB	-0.3~V_{DD}+0.3 Note 1	V
Output voltage	V_{O1}	P00~P06, P10~P17, P30, P31, P40~P43, P50~P55 P60~P63, P70~P77, P120, P130, P136, P140, P141 P146, P147	-0.3~EV_{DD}+0.3 and -0.3~V_{DD}+0.3 Note 1	V
	V_{O2}	P20~P27, P137	-0.3~V_{DD}+0.3 Note 1	V
Analog input voltage	V_{AI1}	ANI8~ANI12	-0.3~EV_{DD}+0.3 and -0.3~AV_{REF} (+) +0.3 Note 1, 2	V
	V_{AI2}	ANI0~ANI7	-0.3~V_{DD}+0.3 and -0.3~AV_{REF}(+)+0.3 Note 1, 2	V

Note1: Not more than 6.5V.

Note2: The pin of the A/ D conversion object cannot exceed AV_{REF}(+)+0.3.

Note: Even if one item in each item instantly exceeds the absolute maximum rating, it may reduce the quality of the product. The absolute maximum rating is the rating that may cause physical damage to the product, and the product must be used in a state that does not exceed the rated value.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. AV_{REF}(+): The positive (+) reference voltage of the A/ D converter
3. Use V_{SS} as the reference voltage.
4. Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

6.3 Absolute Maximum Current Rating

(T_A= -40~125℃)

Item	Symbol	Condition		Rating	Unit
High level output current	I_{OH1}	Each pin	P00~P06, P10~P17, P30, P31, P40~P43, P50~P55 P70~P77, P120, P130, P136, P137, P140, P141 P146, P147	-40	mA
		Pin total -170mA	P00~P04, P40~P43, P120, P130, P136, P137, P140 P141	-70	mA
			P05, P06, P10~P17, P30, P31, P50~P55, P70~P77 P146, P147	-100	mA
	I_{OH2}	Each pin	P20~P27	-3	mA
		Pin total		-15	mA
Low level output current	I_{OL1}	Each pin	P00~P06, P10~P17, P30, P31, P40~P43, P50~P55 P60~P63, P70~P77, P120, P130, P136, P137, P140 P141, P146, P147	40	mA
		The total pins are 170mA	P00~P04, P40~P43, P120, P130, P136, P137, P140 P141	100	mA
			P05, P06, P10~P17, P30,P31, P50~P55, P70~P77 P146, P147	120	mA
	I_{OL2}	Each pin	P20~P27	15	mA
		Pin total		45	mA
Input negative current	I_{INJL}	Each pin	Continuous DC negative current that can be injected into an input pin	-3	mA
		Pin total		-15	mA
Input positive current	I_{INJH}	Each pin	Continuous DC positive current that can be injected into an input pin	3	mA
		Pin total		15	mA
Operating ambient temperature	T_A	Usually runtime		-40~125	℃
		When programming the flash memory			
Storage temperature	T_{stg}	-		-65~150	℃

Note: Even if one item in each item instantly exceeds the absolute maximum rating, it may reduce the quality of the product. The absolute maximum rating is the rating that may cause physical damage to the product, and the product must be used in a state that does not exceed the rated value.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexed pin are the same as the characteristics of the port pin.
2. Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

6.4 Oscillation Circuit Characteristics

6.4.1 X1, XT1 Features

(T_A= -40~125℃, 2.0V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Resonator	Condition	Min	Typ	Max	Unit
X1 clock oscillation frequency (F_X).	Ceramic resonators/ crystal resonators	-	1.0	-	20.0	MHz
X1 clock oscillation stabilization time	Ceramic resonators/ crystal resonators	20MHz, C=10pF	-	15	-	ms
X1 clock oscillation feedback resistor	Ceramic resonators/ crystal resonators	-	0.6	-	1.8	MΩ
XT1 clock oscillation frequency (F_{XT}).	Crystal resonator	-	32	32.768	35	KHz
XT1 clock oscillation stabilization time	Crystal resonator	32.768KHz, C=10pF	-	2	-	s

Note:

1. It only indicates the frequency tolerance range of the oscillation circuit, and the command execution time should refer to the AC characteristics.
2. Please entrust the resonator manufacturer with an evaluation after installing the circuit and use it after checking the oscillation characteristics.

Remark: Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

6.4.2 Internal Oscillator Characteristics

(T_A= -40~125℃,2.0V≤V_{DD}≤5.5V, V_{SS}=0V)

Resonator	Condition	Min	Typ	Max	Unit
Clock frequency (F_{IH}) of high-speed internal oscillator Note 1,2	-	1.0	-	64.0	MHz
High-speed internal oscillator settling time (T_{SU}).	-	-	12	-	us
Clock frequency accuracy of high-speed internal oscillators	T_A= 10~70℃	-1.0	-	+1.0	%
	T_A= 0~105℃	-1. 5	-	+1.5	%
	T_A= -10~125℃	-2.0	-	+2.0	%
	T_A= -40~125℃	-4.0	-	+4.0	%
The clock frequency (F_{IL}) of the low-speed internal oscillator	-	10	15	20	KHz

Note1: Select the frequency of the high-speed internal oscillator via the option byte.

Note2: Only the characteristics of the oscillation circuit are expressed, and the command execution time should refer to the AC characteristics.

Note: Low temperature specification value shall be guaranteed by the design, and low temperature conditions shall not be measured in mass production.

Remark: Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

6.5 DC Characteristics

6.5.1 Pin Characteristics

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High-level output current Note1	I_{OH1}	P00~P06, P10~P17, P30, P31 P40~P43, P50~P55, P70~P77 P120, P130, P136, P137, P140 P141, P146, P147 1 pin alone	2.0V≤EV_{DD}≤5.5V -40~85℃	-	-	-12.0 Note2	mA
			2.0V≤EV_{DD}≤5.5V 85~125℃	-	-	-6.0 Note2	
		P00~P04, P40~P43, P120, P130 P136, P137, P140, P141 Total pins (when duty cycle ≤ 70% Note3)	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	-60.0	mA
			4.0V≤EV_{DD}≤5.5V 85~125℃	-	-	-30.0	
			2.4V≤EV_{DD}<4.0V	-	-	-12.0	mA
			2.0V≤EV_{DD}<2.4V	-	-	-6.0	mA
		P05, P06, P10~P17, P30, P31 P50~P53, P70~P77, P146, P147 Total pins (when duty cycle ≤ 70% Note3)	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	-80.0	mA
			4.0V≤EV_{DD}≤5.5V +85~125℃	-	-	-30.0	
			2.4V≤EV_{DD}<4.0V	-	-	-20.0	mA
			2.0V≤EV_{DD}<2.4V	-	-	-10.0	mA
		Total pins (when duty cycle ≤ 70% Note3)	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	-140.0	mA
			4.0V≤EV_{DD}≤5.5V 85~125℃	-	-	-60.0	
			2.4V≤EV_{DD}≤4.0V	-	-	-30	
			2.0V≤EV_{DD}≤2.4V	-	-	-15	
	I_{OH2}	P20~P27 1 pin alone	2.0V≤V_{DD}≤5.5V	-	-	-2.5 Note2	mA
		Total pins (when duty cycle ≤ 70% Note3)	2.0V≤V_{DD}≤5.5V	-	-	-10	mA

Note1: This is the current value that guarantees the operation of the device even if the current flows from the EV_{DD} and V_{DD} pins to the output pins.

Note2: The total current value cannot be exceeded.

Note3: Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor ＞ 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current of pins = (IOH × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOH = -10.0 mA

Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Note: In N-channel open-drain mode, P00, P02~P04, P10, P11, P13~P15, P17, P30, P50, P51, P55, P71, The P74 does not output a high level (for example, a 64-pin product).

Remark:

1. Unless otherwise specified, the characteristics of the multiplexed pin are the same as the characteristics of the port pin.
2. Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Low level output current Note1	I_{OL1}	P00~P06, P10~P17, P30, P31 P40~P43, P50~P55, P60~P63 P70~P77, P120, P130, P136 P137, P140, P141, P146, P147 1 pin alone	2.0V≤EV_{DD}≤5.5V -40~85℃	-	-	30 Note2	mA
			2.0V≤EV_{DD}≤5.5V 85~125℃	-	-	15 Note2	mA
		P00~P04, P40~P43, P120 P130, P136, P137, P140, P141 Total pins (when duty cycle ≤ 70% Note3)	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	100	mA
			4.0V≤EV_{DD}≤5.5V 85~125℃	-	-	50	mA
			2.4V≤EV_{DD}<4.0V	-	-	30	mA
			2.0V≤EV_{DD}<2.4V	-	-	15	mA
		P05, P06, P10~P17, P30, P31 P50~P55, P60~P63, P70~P77 P146, P147 Total pins (when duty cycle ≤ 70% Note3)	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	120	mA
			4.0V≤EV_{DD}≤5.5V 85~125℃	-	-	60	mA
			2.4V≤EV_{DD}<4.0V	-	-	40	mA
			2.0V≤EV_{DD}<2.4V	-	-	20	mA
		Total of all pins (when duty cycle ≤ 70% Note3)	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	150	mA
			4.0V≤EV_{DD}≤5.5V 85~125℃	-	-	80	mA
			2.4V≤EV_{DD}≤4.0V	-	-	50	mA
			2.0V≤EV_{DD}≤2.4V	-	-	30	mA
	I_{OL2}	P20~P27 1 pin alone	2.0V≤V_{DD}≤5.5V	-	-	6 Note2	mA
		Total of all pins (when duty cycle ≤ 70% Note3)	2.0V≤V_{DD}≤5.5V	-	-	20	mA

Note1: This is the current value that guarantees the operation of the device even if the current flows from the output pin to the EV_{SS} and V_{SS} pins.

Note2: The total current value cannot be exceeded.

Note3: This is the output current value for the "duty cycle≤70% condition".The output current value of 70% ＞can be calculated using the following equation (when the duty cycle is changed to n%.

• Output current of pin total = (I_{OL}×0.7)/ (n×0.01).

＜ calculation example ＞ I_{OL}= 10.0mA, n = 80%

Output current totaled by pins = (10.0×0.7)/ (80×0.01) ≈ 8.7mA

The current at each pin does not vary by duty cycle and does not flow above the absolute maximum rating.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexed pin are the same as the characteristics of the port pin.

2. Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Power supply input voltage	V_{DD} EV_{DD}	-		2.0	-	5.5	V
The input voltage to the power supply ground	V_{SS} EV_{SS}	-		-0.3	-	-	V
High level input voltage	V_{IH1}	P00~P06, P10~P17 P30, P31, P40~P43 P50~P55, P70~P77 P120, P136, P140, P141 P146, P147	Schmidt input	0.8EV_{DD}	-	EV_{DD}	V
	V_{IH2}	P01, P03, P04, P10 P14~P17, P30, P50, P55	TTL input 4.0V≤EV_{DD}≤5.5V	2.2	-	EV_{DD}	V
			TTL input 3.3V≤EV_{DD}<4.0V	2.0	-	EV_{DD}	V
			TTL input 2.0V≤EV_{DD}<3.3V	1.5	-	EV_{DD}	V
	V_{IH3}	P20~P27, P137		0.7V_{DD}	-	V_{DD}	V
	V_{IH4}	P60~P63		0.7EV_{DD}	-	6.0	V
	V_{IH5}	P121~P124, EXCLK, EXCLKS, RESETB		0.8V_{DD}	-	V_{DD}	V
Low level input voltage	V_{IL1}	P00~P06, P10~P17 P30, P31, P40~P43 P50~P55, P70~P77 P120, P136, P140, P141 P146, P147	Schmidt input	0	-	0.2EV_{DD}	V
	V_{IL2}	P01, P03, P04, P10 P14~P17, P30, P50, P55	TTL input 4.0V≤EV_{DD}≤5.5V	0	-	0.8	V
			TTL input 3.3V≤EV_{DD}<4.0V	0	-	0.5	V
			TTL input 2.0V≤EV_{DD}<3.3V	0	-	0.32	V
	V_{IL3}	P20~P27, P137		0	-	0.3V_{DD}	V
	V_{IL4}	P60~P63		0	-	0.3EV_{DD}	V
	V_{IL5}	P121~P124, EXCLK, EXCLKS, RESETB		0	-	0.2V_{DD}	V

Note: Even in N-channel open-drain mode, P00, P02~P04, P10, P11, P13~P15, P17, P30, P50, P51, P55, P71, the maximum V_{IH} (MAX.) of the P74 is also EV_{DD} (for example, a 64-pin product).

Remark:

1. Unless otherwise specified, the characteristics of the multiplexed pin are the same as the characteristics of the port pin.
2. Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High-level output voltage	V_{OH1}	P00~P06, P10~P17, P30 P31, P40~P43, P50~P55 P70~P77, P120, P130 P136, P137, P140, P141 P146, P147	4.0V≤EV_{DD}≤5.5V I_{OH1}= -12.0mA	EV_{DD}-1.5	-	-	V
			4.0V≤EV_{DD}≤5.5V I_{OH1}= -6.0mA	EV_{DD}-0.7	-	-	V
			2.4V≤EV_{DD}≤5.5V I_{OH1}= -3.0mA	EV_{DD}-0.6	-	-	V
			2.0V≤EV_{DD}≤5.5V I_{OH1}= -2mA	EV_{DD}-0.5	-	-	V
	V_{OH2}	P20~P27	4.0V≤V_{DD}≤5.5V I_{OH2}= -2.5mA	EV_{DD}-1.5	-	-	V
			4.0V≤V_{DD}≤5.5V I_{OH2}= -1.5mA	EV_{DD}-0.7	-	-	V
			2.4V≤V_{DD}≤5.5V I_{OH2}= -0.5mA	EV_{DD}-0.6	-	-	V
			2.0V≤V_{DD}≤5.5V I_{OH2}= -0.4mA	V_{DD}-0.5	-	-	V
Low level output voltage	V_{OL1}	P00~P06, P10~P17, P30 P31, P40~P43, P50~P55 P60~P63, P70~P77, P120 P130, P136, P137, P140 P141, P146, P147	4.0V≤EV_{DD}≤5.5V I_{OL1}=30.0mA	-	-	1. 2	V
			4.0V≤EV_{DD}≤5.5V I_{OL1}=15.0mA	-	-	0.7	V
			2.4V≤EV_{DD}≤5.5V I_{OL1}=6.0mA	-	-	0.4	V
			2.0V≤EV_{DD}≤5.5V I_{OL1}=4.0mA	-	-	0.4	V
	V_{OL2}	P20~P27	4.0V≤V_{DD}≤5.5V I_{OL2}=6.0mA	-	-	1. 2	V
			4.0V≤V_{DD}≤5.5V I_{OL2}=4.0mA	-	-	0.7	V
			2.4V≤V_{DD}≤5.5V I_{OL2}=1.5mA	-	-	0.4	V
			2.0V≤V_{DD}≤5.5V I_{OL2}=1.0mA	-	-	0.4	V

Note: In N-channel open-drain mode, P00, P02~P04, P10, P11, P13~P15, P17, P30, P50, P51, P55, P71, The P74 does not output a high level (for example, a 64-pin product).

Remark:

1. Unless otherwise specified, the characteristics of the multiplexed pin are the same as the characteristics of the port pin.
2. Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High-level Input leakage current	I_{LIH1}	P00~P06, P10~P17 P30, P31, P40~P43 P50~P55, P70~P77 P120, P136, P140 P141, P146, P147	V_I=EV_{DD}	-	-	1	μA
	I_{LIH2}	P20~P27, P137 RESETB	V_I=V_{DD}	-	-	1	μA
	I_{LIH3}	P121~P124 (X1, X2 EXCLK, XT1, XT2 EXCLKS)	V_I=V_{DD}, when input port and external clock input	-	-	1	μA
			V_I=V_{DD}, when a resonator is connected	-	-	10	μA
Low Input leakage current	I_{LIL1}	P00~P06, P10~P17 P30, P31, P40~P43 P50~P55, P70~P77 P120, P136, P140 P141, P146, P147	V_I=EV_{SS}	-	-	-1	μA
	I_{LIL2}	P20~P27, P137 RESETB	V_I=V_{SS}	-	-	-1	μA
	I_{LIL3}	P121~P124 (X1, X2 EXCLK, XT1, XT2 EXCLKS)	V_I=V_{SS}, when the input port and the external clock are entered	-	-	-1	μA
			V_I=V_{SS}, when a resonator is connected	-	-	-10	μA
Internal pull-up resistor	R_U	P00~P06, P10~P17 P30, P31, P40~P43 P50~P55, P70~P77 P120, P136, P137 P140, P141, P146 P147	V_I=EV_{SS}, when entering the port	10	30	100	KΩ

Note: Unless otherwise specified, the characteristics of the multiplexed pin are the same as the characteristics of the port pin.

Remark: Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

6.5.2 Supply Current Characteristics

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition				Min	Typ	Max	Unit
Supply current Note1	I_{DD1}	Run mode	High-speed internal oscillator	F_{HOCO}=64MHz, F_{IH}=32MHz Note3		-	4.6	10.5	mA
				F_{HOCO}=48MHz, F_{IH}=48MHz Note3		-	4.9	11.5	
				F_{HOCO}=32MHz, F_{IH}=32MHz Note3		-	4.4	9.0	
			High-speed master system clock	F_{MX}=20MHz Note2	Enter a square wave	-	2.3	5.4	mA
					Connect the crystal	-	2.3	5.4	
			The secondary system clock runs	F_{SUB}=32.768Khz Note4	Enter a square wave	-	70	120	uA
					Connect the crystal	-	70	120	
	I_{DD2}	Sleep mode	High-speed internal oscillator	F_{HOCO}=64MHz, F_{IH}=32MHz Note3		-	1.2	5.8	mA
				F_{HOCO}=48MHz, F_{IH}=48MHz Note3		-	1.2	6.5	
				F_{HOCO}=32MHz, F_{IH}=32MHz Note3		-	1.2	4.5	
			High-speed master system clock	F_{MX}=20Mhz Note2	Enter a square wave	-	0.7	2.0	mA
					Connect the crystal	-	0.7	2.0	
			The secondary system clock runs	F_{SUB}=32.768KHz Note5	Enter a square wave	-	0.7	40	uA
					Connect the crystal	-	0.7	40	
	I_{DD3}	Deep Sleep Mode Note7	T_A= -40℃~25℃, V_{DD}=3.0V			-	0.45	1.1	uA
			T_A= -40℃~85℃, V_{DD}=3.0V			-	0.45	8.0	
			T_A= -40℃~105℃, V_{DD}=3.0V			-	0.45	12.5	
			T_A= -40℃~125℃, V_{DD}=3.0V			-	0.45	35	

Note1: This is the total current through V_{DD} and EV_{DD}, including input leakage current fixed to V_{DD}, EV_{DD}, or V_{SS}, EV_{SS} on the input pin. Typical alue: CPU is multiplied. Algorithm instruction execution (I_{DD1}) and does not include external operating current. Maximum Value: The CPU is in multiply instruction execution (I_{DD1}) and contains external operating current, but does not include current to the A/ D converter, LVD circuitry, I/ O ports, and internal pull-up or pull-down resistors, nor does it include the current when overwriting the data flash memory.

Note2: This is when the high-speed internal oscillator and the subsystem clock stop oscillating.

Note3: This is when the high-speed primary and secondary system clocks stop oscillating.

Note4: This is when the high-speed internal oscillator and the high-speed main system clock stop oscillating.

Note5: This is when the high-speed internal oscillator and the high-speed main system clock stop oscillating. Contains current to the RTC, but does not include current to 15-bit interval timers and watchdog timers.

Note6: Current to RTC, 15-bit interval timers, and watchdog timers is not included.

Note7: For the current value when the secondary system clock is running in deep sleep mode, refer to the current value when the secondary system clock is running in sleep mode.

Remark:

1. F_{HOCO}: The clock frequency of the high-speed internal oscillator, F_{IH}: The system clock frequency provided by the high-speed internal oscillator.
2. F_{SUB}: External subsystem clock frequency (XT1/ XT2 clock oscillation frequency).
3. F_{MX}: External main system clock frequency (X1/ X2 clock oscillation frequency).
4. TYP. The temperature condition of the value is T_A=25℃.
5. Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Low speed internal oscillator operating current	I_{FIL} Note 1	-		-	0.2	-	uA
RTC operating current	I_{RTC} Note1,2,3	-		-	0.04	-	uA
15-bit interval timer operating current	I_{IT} Note1,2,4	-		-	0.02	-	uA
Watchdog timer operating current	I_{WDT} Note1,2,5	F_{IL}=15KHz		-	0.22	-	uA
A/D converter operating current	I_{ADC} Note 1, 6	ADC HS mode @ 64MHz		-	2. 2	-	mA
		ADC HS mode @ 4MHz		-	1. 3	-	mA
		ADC LC mode @ 24MHz		-	1.1	-	mA
		ADC LC mode @ 4MHz		-	0.8	-	mA
D/A converter operating current	I_{DAC} Note1,8	Per channel		-	1.4	-	mA
PGA operating current		Per channel		-	480	700	uA
Comparator operating current	I_{CMP} Note1,9	Per channel	No internal reference voltage is used	-	60	100	uA
			An internal reference voltage is used	-	80	140	uA
LVD operating current	I_{LVD} Note1,7	-		-	0.08	-	uA

Note1: This is the current flowing through V_{DD}.

Note2: This is when the high-speed internal oscillator and the high-speed system clock stop oscillating.

Note3: This is the current that flows only to the real-time clock (RTC) (excluding the operating current of the low-speed internal oscillator and the XT1 oscillation circuit). In the case of a real-time clock operating in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{RTC} value. In addition, I_{FIL} must be added when selecting a low-speed internal oscillator. I_{DD2} when the secondary system clock is running contains the operating current of the real-time clock.

Note4: This is the current that flows only to the 15-bit interval timer (excluding the operating current of the low-speed internal oscillator and XT1 oscillation circuit). In the case of 15-bit interval timer operation in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{IT} value. In addition, I_{FIL} must be added when selecting a low-speed internal oscillator.

Note5: This is the current that flows only to the watchdog timer (including the operating current of the low-speed internal oscillator). In the case of watchdog timer operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus I_{WDT}.

Note6: This is the current that only flows to the A/ D converter. In the case of A/ D converter operation in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{ADC} value.

Note7: This is the current that only flows to the LVD circuit. In the case of LVD circuit operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the value of I_{LVD}.

Note8: This is the current that only flows to the D/ A converter. In the case of D/ A converter operation in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{DAC} value.

Note9: This is the current that only flows to the comparator circuit. In the case of comparator circuit operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the I_{CMP} value.

Remark:

1. F_{IL}: The clock frequency of the low-speed internal oscillator
2. TYP. The temperature condition of the value is T_A=25℃.
3. Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

6.6 AC Characteristics

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	The main system clock (F_{MAIN}) is running	2.0V≤V_{DD}≤5.5V	0.02084	-	1	us
		The secondary system clock (F_{SUB}) runs	2.0V≤V_{DD}≤5.5V	28.5	30.5	31.3	us
External system clock frequency	F_{EX}	2.0V≤V_{DD}≤5.5V		1.0	-	20.0	MHz
	F_{EXS}	2.0V≤V_{DD}≤5.5V		32.0	-	35.0	KHz
The high and low width of the external system clock input	T_{EXH}, T_{EXL}	2.0V≤V_{DD}≤5.5V		24	-	-	ns
	T_{EXHS}, T_{EXLS}	2.0V≤V_{DD}≤5.5V		13.7	-	-	us
TI00 ~ TI03, input high and low level width	T_{TIH}, T_{TIL}	2.0V≤V_{DD}≤5.5V		1/ F_{MCK}+10	-	-	ns
The input period of the timer TimerA	T_C	TAIO	2.4V≤EV_{DD}≤5.5V	100	-	-	ns
			2.0V≤EV_{DD}<2.4V	300	-	-	ns
The high and low width of the timer TimerA input	T_{TAIH}, T_{TAIL}	TAIO	2.4V≤EV_{DD}≤5.5V	40	-	-	ns
			2.0V≤EV_{DD}<2.4V	120	-	-	ns

Note: F_{MCK}: The operating clock frequency of the Timer4 unit

Remark: Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
The high and low width of the timer M input	T_{TMIH}, T_{TMIL}	TMIOA0, TMIOA1, TMIOB0 TMIOB1, TMIOC0, TMIOC1 TMIOD0, TMIOD1		3/ F_{CLK}	-	-	ns
Timer M forces the low width of the cutoff signal input	T_{TMSIL}	P136/ INTP0	2MHz<F_{CLK}≤48MHz	1	-	-	us
			F_{CLK}≤2MHz	1/ F_{CLK}+1	-	-	us
The high and low width of the timer B input	T_{TBIH}, T_{TBIL}	TBIOA, TBIOB		2.5/ F_{CLK}	-	-	ns
Output frequency of TO00 ~ TO03, TAIO0, TAO0, TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1, TBIOA, TBIOB	F_{TO}	4.0V≤EV_{DD}≤5.5V		-	-	16	MHz
		2.4V≤EV_{DD}<4.0V		-	-	8	MHz
		2.0V≤EV_{DD}<2.4V		-	-	4	MHz
Output frequency of CLKBUZ0, CLKBUZ1	F_{PCL}	4.0V≤EV_{DD}≤5.5V		-	-	16	MHz
		2.4V≤EV_{DD}<4.0V		-	-	8	MHz
		2.0V≤EV_{DD}<2.4V		-	-	4	MHz
The high and low width of the interrupt input	T_{INTH}, T_{INTL}	INTP0~INT P11	2.0V≤EV_{DD}≤5.5V	1	-	-	us
Key to interrupt the high and low width of the input	T_{KR}	KR0~KR7	2.0V≤EV_{DD}≤5.5V	250	-	-	ns
The low-level width of RESETB	T_{RSL}	-		10	-	-	us

Remark: Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

6.7 Peripheral Features

6.7.1 Universal Interface Unit

(1) UART Mode

(T_A= -40~85℃,2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Condition		Specification value		Unit
			Min	Max	
Transfer rate	2.0V ≤ EV_{DD} ≤ 5.5V	-	-	F_{MCK}/ 6	bps
		The theoretical value of the maximum transmission rate f_{MCK} = f_{CLK}	-	8	Mbps

(T_A=85~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Condition		Specification value		Unit
			Min	Max	
Transfer rate	2.0V ≤ EV_{DD} ≤ 5.5V	-	-	F_{MCK}/ 12	bps
		The theoretical value of the maximum transmission rate f_{MCK} = f_{CLK}	-	4	Mbps

Remark: It is guaranteed by the design and not tested in mass production.

(2) Three-wire SPI mode (master mode, internal clock output).

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		-40~85℃		85~125℃		Unit
				Min	Max	Min	Max	
SCLKP cycle time	T_{KCY1}	T_{KCY1} ≥ 2/ F_{CLK}	4.0V≤EV_{DD}≤5.5V	41.67	-	83.33	-	ns
			2.7V≤EV_{DD}≤5.5V	83.33	-	166.67	-	ns
			2.4V≤EV_{DD}≤5.5V	125	-	250	-	ns
			2.0V≤EV_{DD}≤5.5V	250	-	500	-	ns
SCLKp high/ low level width	T_{KH1},T_{KL1}	4.0V≤EV_{DD}≤5.5V		T_{KCY1}/ 2-7	-	T_{KCY1}/ 2-14	-	ns
		2.7V≤EV_{DD}≤5.5V		T_{KCY1}/ 2-10	-	T_{KCY1}/ 2-20	-	ns
		2.4V≤EV_{DD}≤5.5V		T_{KCY1}/ 2-18	-	T_{KCY1}/ 2-36	-	ns
		2.0V≤EV_{DD}≤5.5V		T_{KCY1}/ 2-38	-	T_{KCY1}/ 2-76	-	ns
SDIp preparation time (to SCLKp↑).	T_{SIK1}	4.0V≤EV_{DD}≤5.5V		23	--	46	-	ns
		2.7V≤EV_{DD}≤5.5V		33		66	-	ns
		2.4V≤EV_{DD}≤5.5V		44	-	88	-	ns
		2.0V≤EV_{DD}≤5.5V		75	-	113	-	ns
SDIp hold time (vs. SCLKp↑)	T_{KSI1}	2.0V≤EV_{DD}≤5.5V		10	-	20	-	ns
SCLKp↓→ SDOp output delay time	T_{KSO1}	2.0V≤EV_{DD}≤5.5V C=20pF Note1		-	10	-	20	ns

Note1: C is the load capacitance of the SCLKp, SDOp output lines.

Note: The SDIp pin is selected as the usual input buffer and the SDOp pin and SCLKp pin as the usual output mode via the port input mode register and the port output mode register.

Remark: It is guaranteed by the design and not tested in mass production.

(3) Three-wire SPI mode (slave mode, external clock input).

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		-40~85℃		85~125℃		Unit
				Min	Max	Min	Max	
SCLKp cycle time	T_{KCY2}	4.0V ≤EV_{DD} ≤ 5.5V	20MHz＜F_{MCK}	8/ F_{MCK}	-	16/ F_{MCK}	-	ns
			F_{MCK} ≤20MHz	6/ F_{MCK}	-	12/ F_{MCK}	-	ns
		2.7V ≤EV_{DD} ≤ 5.5V	16MHz ＜F_{MCK}	8/ F_{MCK}	-	16/ F_{MCK}	-	ns
			F_{MCK} ≤16MHz	6/ F_{MCK}	-	12/ F_{MCK}	-	ns
		2.4V ≤EV_{DD} ≤ 5.5V		6/ F_{MCK} and≥500	-	12/ F_{MCK} and≥1000	-	ns
		2.0V ≤EV_{DD} ≤ 5.5V		6/ F_{MCK} and≥750	-	12/ F_{MCK} and≥1500	-	ns
SCLKp high/ low level width	T_{KH2} T_{KL2}	4.0V ≤EV_{DD} ≤ 5.5V		T_{KCY1}/ 2-7	-	T_{KCY1}/ 2-14	-	ns
		2.7V ≤EV_{DD} ≤ 5.5V		T_{KCY1}/ 2-8	-	T_{KCY1}/ 2-16	-	ns
		2.0V ≤EV_{DD} ≤ 5.5V		T_{KCY1}/ 2-18	-	T_{KCY1}/ 2-36	-	ns
SDIp preparation time (to SCLKp↑)	T_{SIK2}	2.7V ≤EV_{DD} ≤ 5.5V		1/ F_{MCK}+20	-	1/ F_{MCK} +40	-	ns
		2.0V ≤EV_{DD} ≤ 5.5V		1/ F_{MCK}+30	-	1/ F_{MCK} +60	-	ns
SDIp hold time (vs. SCLKp↑)	T_{KSI2}	2.0V ≤EV_{DD} ≤ 5.5V		1/ F_{MCK}+31	-	1/ F_{MCK} +62	-	ns
SCLKp↓ → SDOp output delay time	T_{KSO2}	2.7V ≤EV_{DD} ≤ 5.5V C=30pF Note1		-	2/ F_{MCK}+44	-	2/ F_{MCK}+66	ns
		2.4V ≤EV_{DD} ≤ 5.5V C=30pF Note1		-	2/ F_{MCK}+75	-	2/ F_{MCK}+113	ns
		2.0V ≤EV_{DD} ≤ 5.5V C=30pF Note1		-	2/ F_{MCK}+100	-	2/ F_{MCK}+150	ns

Note1: C is the load capacitance of the SCLKp and SDOp output lines.

Note: Select the SDIp pin and SCLKp pin as the usual input buffer and the SDOp pin as the usual output mode via the port input mode register and the port output mode register.

Remark: It is guaranteed by the design and not tested in mass production.

(4) Four-wire SPI mode (slave mode, external clock input).

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		-40~85℃		85~125℃		Unit
				Min	Max	Min	Max	
SSI00 settling time	T_{SSIK}	DAPmn=0	2.7V ≤EV_{DD}≤ 5.5V	120	-	240	-	ns
			2.0V ≤EV_{DD}≤ 5.5V	200	-	400	-	ns
		DAPmn=1	2.7V ≤EV_{DD}≤ 5.5V	1/ F_{MCK}+120	-	1/ F_{MCK}+240	-	ns
			2.0V ≤EV_{DD}≤ 5.5V	1/ F_{MCK}+200	-	1/ F_{MCK}+400	-	ns
SSI00 hold time	T_{KSSI}	DAPmn=0	2.7V ≤EV_{DD}≤ 5.5V	1/ F_{MCK}+120	-	1/ F_{MCK}+240	-	ns
			2.0V ≤EV_{DD}≤ 5.5V	1/ F_{MCK}+200	-	1/ F_{MCK}+400	-	ns
		DAPmn=1	2.7V ≤EV_{DD}≤ 5.5V	120	-	240	-	ns
			2.0V ≤EV_{DD}≤ 5.5V	200	-	400	-	ns

Note: Select the SDIp pin and SCLKp pin as the usual input buffer and the SDOp pin as the usual output mode via the port input mode register and the port output mode register.

Remark: It is guaranteed by the design and not tested in mass production.

(5) Simple IIC mode

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	-40~85℃		85~125℃		Unit
			Min	Max	Min	Max	
SCLr clock frequency	F_{SCL}	2.7V ≤EV_{DD}≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	-	1000 Note1	-	400 Note1	KHz
		2.0V ≤EV_{DD}≤ 5.5V C_b = 100 pF, R_b = 3KΩ	-	400 Note1	-	100 Note1	KHz
		2.0V ≤EV_{DD}≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	-	300 Note1	-	75 Note1	KHz
When SCLr is low hold time	T_{LOW}	2.7V ≤EV_{DD}≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	475	-	1200	-	ns
		2.0V ≤EV_{DD}≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	1150	-	4600	-	ns
		2.0V ≤EV_{DD}≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1550	-	6500	-	ns
When SCLr is high hold time	T_{HIGH}	2.7V ≤EV_{DD}≤ 5.5V C_b = 50 pF, R_b = 2.7KΩ	475	-	1200	-	ns
		2.0V ≤EV_{DD}≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	1150	-	4600	-	ns
		2.0V ≤EV_{DD}≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1550	-	6500	-	ns
Data settling time (receiving)	$T_{SU:DAT}$	2.7V ≤EV_{DD}≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	1/ F_{MCK}+85 Note2	-	1/ F_{MCK}+220 Note2	-	ns
		2.0V ≤EV_{DD}≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	1/ F_{MCK}+145 Note2	-	1/ F_{MCK}+580 Note2	-	ns
		2.0V ≤EV_{DD}≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1/ F_{MCK}+230 Note2	-	1/ F_{MCK}+1200 Note2	-	ns
Data retention time (sending)	$T_{HD:DAT}$	2.7V ≤EV_{DD}≤ 5.5V C_b = 50 pF, R_b = 2.7KΩ	-	305	-	770	ns
		2.0V ≤EV_{DD}≤ 5.5V C_b = 100 pF, R_b = 3KΩ	-	355	-	1420	ns
		2.0V ≤EV_{DD}≤ 2.7V C_b = 100 pF, R_b = 5KΩ	-	405	-	2070	ns

Note1: Must be set to at least F_{MCK}/ 4.

Note2: The f_{MCK} setting cannot exceed the hold time of SCLr="L" and SCLr="H".

Remark: It is guaranteed by the design and not tested in mass production.

6.7.2 Serial Interface IICA

1) I^2C standards mode

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min	Max	
SCLA0 clock frequency	F_{SCL}	Standard mode: F_{CLK}≥1MHz	-	100	KHz
The time when the start condition was established	$T_{SU:STA}$	-	4.7	-	us
Hold time of the start condition Note 1	$T_{HD:STA}$	-	4.0	-	us
When SCLA0 is low hold time	T_{LOW}	-	4.7	-	us
When SCLA0 is high hold time	T_{HIGH}	-	4.0	-	us
Data settling time (receiving)	$T_{SU:DAT}$	-	250	-	ns
Data retention time (sending) Note 2	$T_{HD:DAT}$	-	0	3.45	us
The time when the stop condition was established	$T_{SU:STO}$	-	4.0	-	us
Bus idle time	T_{BUF}	-	4.7	-	us

Note1: Generate the first clock pulse after generating a start condition or a restart condition.

Note2: During normal transmission, it is necessary to ensure the maximum of $T_{HD:DAT}$ (Max.), and it is necessary to wait when the reply (ACK) is performed.

Note: The maximum. value of C_b (communication line capacitance) and R_b (communication line pull-up resistance value) for each mode are as follows:

Standard mode: C_b=400pF, R_b=2.7kΩ.

Remark: It is guaranteed by the design and not tested in mass production.

2) I²C fast mode

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min	Max	
SCLA0 clock frequency	F_{SCL}	Fast mode: F_{CLK}≥3.5MHz	-	400	KHz
The time when the start condition was established	$T_{SU:STA}$	-	0.6	-	us
Hold time of the start condition Note 1	$T_{HD:STA}$	-	0.6	-	us
When SCLA0 is low hold time	T_{LOW}	-	1.3	-	us
When SCLA0 is high hold time	T_{HIGH}	-	0.6	-	us
Data settling time (receiving)	$T_{SU:DAT}$	-	100	-	ns
Data retention time (sending) Note 2	$T_{HD:DAT}$	-	0	0.9	us
The time when the stop condition was established	$T_{SU:STO}$	-	0.6	-	us
SCLA0 clock frequency	T_{BUF}	-	1.3	-	us

Note1: Generate the first clock pulse after generating a start condition or a restart condition.

Note2: The maximum of $T_{HD:DAT}$ (Max.) needs to be guaranteed during normal transmission, and it is necessary to wait for the acknowledgment (ACK).

Note: The maximum. value of C_b (communication line capacitance) and R_b (communication line pull-up resistance value) for each mode are as follows:

Fast mode: C_b=320pF, R_b=1.1kΩ

Remark: It is guaranteed by the design and not tested in mass production.

3) I²C Enhanced Fast Mode

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min	Max	
SCLA0 clock frequency	F_{SCL}	Enhanced Fast Mode: F_{CLK}≥10MHz	-	1000	KHz
The time when the start condition was established	$T_{SU:STA}$	-	0.26	-	us
Hold time of the start condition Note 1	$T_{HD:STA}$	-	0.26	-	us
When SCLA0 is low hold time	T_{LOW}	-	0.5	-	us
When SCLA0 is high hold time	T_{HIGH}	-	0.26	-	us
Data settling time (receiving)	$T_{SU:DAT}$	-	50	-	ns
Data retention time (sending) Note 2	$T_{HD:DAT}$	-	0	0.45	us
The time when the stop condition was established	$T_{SU:STO}$	-	0.26	-	us
Bus idle time	T_{BUF}	-	0.5	-	us

Note1: Generate the first clock pulse after generating a start condition or a restart condition.

Note2: During normal transmission, it is necessary to ensure the maximum of $T_{HD:DAT}$ (MAX.), and wait for the acknowledgment (ACK).

Note: The maximum. value of C_b (communication line capacitance) and R_b (communication line pull-up resistance value) for each mode are as follows:

Enhanced fast mode: C_b=120pF, R_b=1.1kΩ.

Remark: It is guaranteed by the design and not tested in mass production.

6.8 Analog Characteristics

6.8.1 A/D Converter Characteristics

Differentiation of A/ D converter characteristics

Input channel \ Reference voltage	Reference voltage (+) =AV_{REFP} Reference voltage (-) =AV_{REFM}	Reference voltage (+) =V_{DD} Reference voltage (-) =V_{SS}
ANI0~ ANI15	Refer to 6.8.1 (1)	Refer to 6.8.1 (2)
Internal reference, the output voltage of the temperature sensor		

(1) Select the case where reference voltage (+) =AV_{REFP}/ ANI0 and reference voltage (-)=AV_{REFM}/ ANI1 are selected

(T_A= -40~125℃,2.0V≤AV_{REFP}≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=0V, Reference voltage (+)=AV_{REFP}, Reference voltage (-) = AV_{REFM} =0V)

Item	Symbol	Condition		Min	Typ	Max	unit
resolution	RES	-		-	12	-	bit
Combined error Note1	ET	12-bit resolution	2.0V ≤ AV_{REFP}≤ 5.5V	-	3	-	LSB
Zero scale error Note1	E_{ZS}	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Full scale error Note1	E_{FS}	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Integral linearity error Note1	EL	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-1	-	1	LSB
Differential Linearity Error Note1	ED	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-1.5	-	1.5	LSB
Conversion time Note3	T_{CONV}	12-bit resolution Conversion object: ANI2~ANI15	2.0V ≤V_{DD}≤ 5.5V	45	-	-	1/ F_{ADC}
		12-bit resolution Conversion object: internal reference voltage, temperature sensor output voltage, PGA output voltage	2.0V ≤V_{DD}≤ 5.5V	72	-	-	1/ F_{ADC}
External input resistors	R_{AIN}	R_{AIN} ＜(Ts/ (F_{ADC} x C_{ADC} x ln(2^{12+2}))- R_{ADC})		-	10 Note4	-	KΩ
Sampling switch resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample-and-hold capacitance	C_{ADC}	-		-	2	-	pF
Analog input voltage	V_{AIN}	ANI2~ANI15		0	-	AV_{REF}	V
		Internal reference voltage(2.0V≤V_{DD}≤5.5V)		V_{BGR} Note2			V
		The output voltage of the temperature sensor (2.0V≤V_{DD}≤5.5V)		V_{TMPS25} Note2			V

Note1: Quantization error (±1/ 2 LSB) is not included.

Note2: Please refer to " 6.8.2 Characteristics of Temperature Sensor/ Internal Reference Voltage".

Note3: F_{ADC} is the operating frequency of AD, and the maximum operating frequency is 48MHz.

Note4: Guaranteed by design, mass production is not tested. TYP are the default sampling period Ts=13.5 and the conversion speed is calculated at F_{ADC}=48MHz.

Remark: It is guaranteed by the design and not tested in mass production.

(2) Select the case where reference voltage (+) =V_{DD} and reference voltage (-) =V_{SS} are selected (T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V,Reference Voltage(+)=V_{DD}, Reference Voltage(-) =V_{SS})

Item	Symbol	Condition		Min	Typ	Max	Unit
resolution	RES	-		-	12	-	bit
Combined error Note1	ET	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-	6	-	LSB
Zero scale error Note1	E_{ZS}	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-	0	-	LSB
Full scale error Note1	E_{FS}	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-	0	-	LSB
Integral linearity error Note1	EL	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-2	-	2	LSB
Differential Linearity Error Note1	ED	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-3	-	3	LSB
Conversion time Note3	T_{CONV}	12-bit resolution Conversion object: ANI0~ ANI15	2.0V≤V_{DD}≤5.5V	45	-	-	1/ F_{ADC}
		12-bit resolution Conversion objects: internal reference voltage, temperature sensor output voltage, PGA output voltage	2.0V≤V_{DD}≤5.5V	72	-	-	1/ F_{ADC}
External input resistors	R_{AIN}	R_{AIN} <(T_S/ (F_{ADC} x C_{ADC} x ln(2^{12+2}))- R_{ADC})		-	10 Note4	-	KΩ
Sampling switch resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample-and-hold capacitance	C_{ADC}	-		-	2	-	pF
Analog input voltage	V_{AIN}	ANI0~ANI7		0	-	V_{DD}	V
		ANI8~ANI15		0	-	EV_{DD}	V
		Internal reference voltage (2.0V≤V_{DD}≤5.5V)		V_{BGR} Note2			V
		The output voltage of the temperature sensor (2.0V≤V_{DD}≤5.5V)		V_{TMPS25} Note2			V

Note1: Quantization error (±1/ 2 LSB) is not included.

Note2: Please refer to " 6.8.2 Characteristics of Temperature Sensor/ Internal Reference Voltage".

Note3: F_{ADC} is the operating frequency of AD, and the maximum operating frequency is 48MHz.

Note4: Guaranteed by design, mass production is not tested. TYP are the default sampling period Ts=13.5 and the conversion speed is calculated at F_{ADC}=48MHz.

Remark: It is guaranteed by the design and not tested in mass production.

6.8.2 Characteristics of the Temperature Sensor/Internal Reference

(T_A= -40~125℃,2.0V≤V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
The output voltage of the temperature sensor	V_{TMPS25}	T_A=25℃	-	1.09	-	V
Internal reference voltage	V_{BGR}	T_A= -40~10℃	1.25	1.45	1.65	V
		T_A=10~70℃	1.38	1.45	1.52	V
		T_A=70~125℃	1.35	1.45	1.55	V
Temperature coefficient	F_{VTMPS}	-	-	-3.5	-	mV/ ℃
Run stable wait time	T_{AMP}	-	5	-	-	us

Remark: Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

6.8.3 D/A Converter

(T_A= -40~125℃,2.0V≤EV_{DD} =V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
resolution	RES	-	-	-	-	8	bit
Combined error	ET	Rload=4MΩ	2.0V≤V_{DD}≤5.5V	-2.5	-	2.5	LSB
Stabilization time	T_{SET}	Cload=20pF	2.7V≤V_{DD}≤5.5V	-	-	3	us
			2.0V≤V_{DD}<2.7V	-	-	6	us
Output impedance	RO	Rload=4MΩ	2.0V≤V_{DD}≤5.5V	4.7	-	8	KΩ

Remark: Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

6.8.4 Comparator

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Input offset voltage	V_{OFFSET}	-		-	±10	±40	mV
Input voltage range	V_{IN}	-		0	-	V_{DD}	V
Internal reference deviation	ΔV_{IREF}	CmRVM register: 7FH~80H(m=0,1)		-	-	±2	LSB
		other		-		±1	LSB
Response time	T_{CR}, T_{CF}	Input amplitude±100mV		-	70	125	ns
Run settling time Note1	T_{STB}	CMPn=0->1	V_{DD}=3.3~5.5V	-	-	1	us
			V_{DD}=2.0~3.3V	-	-	3	
Reference voltage settling time	T_{VR}	CVRE=0->1 Note2		-	-	20	us
Operating current	I_{CMPDD}	Refer to 6.5.2 Supply current characteristics					

Note1: Time from comparator action enable (CMPnEN=0 —>1) to meet various DC/ AC specifications of the CMP.

Note2: Internal reference generator enabled (by setting the CVREm bit to 1; m = 0 to 1), the reference settling time elapses before the comparator output (CnOE bit = 1; n = 0 to 1)

Remark: It is guaranteed by the design and not tested in mass production.

6.8.5 Programmable Gain Amplifier PGA

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Input deviation voltage	V_{IOPGA}	-		-	±3	±10	mV
Input voltage range	V_{IPGA}	-		0	-	0.9xV_{DD}/ Gain	V
Output voltage range	V_{IOHPGA}	-		0.93xV_{DD}	-	-	V
	V_{IOLPGA}	-		-	-	0.07xV_{DD}	V
Gain deviation	EG	x4	-	-	-	±1	%
		x8	-	-	-	±1	%
		x10	-	-	-	±1	%
		x12	-	-	-	±2	%
		x14	-	-	-	±2	%
		x16	-	-	-	±2	%
		x32	-	-	-	±3	%
Slew rate Note2	SR_{RPGA}	Rising Vin= 0.1V_{DD}/ gain to 0.9V_{DD}/ gain. 10 to 90% output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5	-	-	V/ us
			4.0 V ≤ V_{DD} ≤ 5.5 V(x32)	3.0	-	-	
			2.0 V ≤ V_{DD} ≤ 4.0V	0.5	-	-	
	SR_{FPGA}	Falling Vin= 0.1V_{DD}/ gain to 0.9V_{DD}/ gain. 90 to 10% output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5	-	-	
			4.0 V ≤ V_{DD} ≤ 5.5 V(x32)	3.0	-	-	
			2.0 V ≤ V_{DD} ≤ 4.0V	0.5	-	-	
Run settling time Note 1	T_{PGA}	x4	-	-	-	5	us
		x8	-	-	-	5	us
		x10	-	-	-	5	us
		x12	-	-	-	10	us
		x14	-	-	-	10	us
		x16	-	-	-	10	us
		x32	-	-	-	10	us
Operating current	I_{PGADD}	Refer to 6.5.2 Supply current characteristics					

Note1: The time required from PGA action enable (PGAEN=1) to meeting the requirements of each DC and AC specification of the PGA

Note2: Guaranteed by design, mass production is not tested.

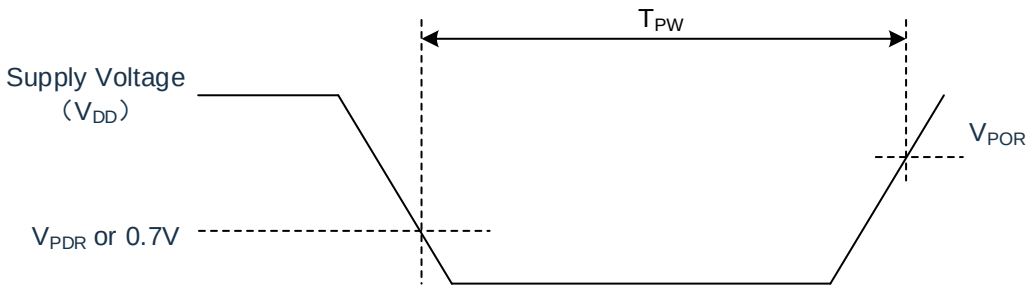
Remark: It is guaranteed by the design and not tested in mass production.

6.8.6 POR Circuit Characteristics

(T_A= -40~125℃, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Detect voltage	V_{POR}	When the supply voltage rises	-	1.50	2.0	V
	V_{PDR}	When the supply voltage drops	1.37	1.45	-	V
Minimum pulse width Note1	T_{PW}	-	300	-	-	us

Note1: This is the time it takes for the POR to reset when V_{DD} is below V_{PDR}. In addition, bit0 (HIOSTOP) and bit7 () of the clock operating state control register (CSC) are set in deep sleep mode MSTOP) stops oscillating the main system clock (F_{AIN}) from V_{DD} below 0.7V until it rises above V_{POR} the time required for reset.



Remark: It is guaranteed by the design and not tested in mass production.

6.8.7 LVD Circuit Characteristics

(1) Reset mode, interrupt mode

(T_A= -40~125℃,V_{PDR}≤V_{DD}≤5.5V,V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Detecting voltage	V_{LVD0}	When the supply voltage rises	-	4.06	4.26	V
		When the supply voltage drops	3.78	3.98	-	V
	V_{LVD1}	When the supply voltage rises	-	3.75	-	V
		When the supply voltage drops	-	3.67	-	V
	V_{LVD2}	When the supply voltage rises	-	3.02	-	V
		When the supply voltage drops	-	2.96	-	V
	V_{LVD3}	When the supply voltage rises	-	2.71	-	V
		When the supply voltage drops	-	2.65	-	V
	V_{LVD4}	When the supply voltage rises	-	2.09	2.16	V
		When the supply voltage drops	1.97	2.04	-	V
The minimum pulse width	T_{LW}	-	300	-	-	us
Detection delay	-	-	-	-	300	us

Remark: It is guaranteed by the design and not tested in mass production.

(2) Interrupt & Reset mode

(T_A= -40~125℃,V_{PDR} ≤V_{DD}≤5.5V,V_{SS}=0V)

Item	Symbol	Condition			Min	Typ	Max	Unit
Interrupt & Reset mode	V_{LVDB0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=1	drop the reset voltage		1.78	1.84	-	V
	V_{LVDB2}		LVIS1=0 LVIS0=1	Rise the reset release voltage	-	2.09	2.16	V
				Drop interrupt voltage	1.97	2.04	-	V
	V_{LVDC0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=0	drop the reset voltage		-	2.45	-	V
	V_{LVDC2}		LVIS1=0 LVIS0=1	Rise the reset release voltage	-	2.71	-	V
				Drop interrupt voltage	-	2.65	-	V
	V_{LVDC3}		LVIS1=0 LVIS0=0	Rise the reset release voltage	-	3.75	-	V
				Drop interrupt voltage	-	3.67	-	V
	V_{LVDD0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=1	drop the reset voltage		--	2.75	-	V
	V_{LVDD2}		LVIS1=0 LVIS0=1	Rise the reset release voltage	-	3.02		V
				Drop interrupt voltage	-	2.96		V
	V_{LVDD3}		LVIS1=0 LVIS0=0	Rise the reset release voltage	-	4.06	4.26	V
				Drop interrupt voltage	3.78	3.98	-	V

Remark: It is guaranteed by the design and not tested in mass production.

6.8.8 Rise Slope Characteristics of Reset Time and Supply Voltage

(T_A= -40~125℃, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Reset time	T_{RESET}	-	-	1	-	ms
The rising slope of the supply voltage	S_{VDD}	-	-	-	54	V/ ms

Remark: It is guaranteed by the design and not tested in mass production.

6.9 Memory Characteristics

6.9.1 Flash Memory

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Symbol	Parameter	Conditions	Min	Max	Unit
T_{PROG}	Word write time (32bit).	T_A= -40~125℃	24	30	us
T_{ERASE}	Sector erase time	T_A= -40~125℃	4	5	ms
	Slice erasure time	T_A= -40~125℃	20	40	ms
N_{END}	Number of erased writes	T_A= -40~125℃	20	-	kcycle
T_{RET}	How long the data is kept	100 kcycle[Note1] at T_A =125℃	20	-	Years

Note1: Full temperature range cycling test.

Note: Guaranteed by design, mass production is not tested.

6.9.2 RAM Memory

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{RAMHOLD}$	RAM holds voltage	T_A= -40~125℃	0.8	-	V

Remark: It is guaranteed by the design and not tested in mass production.

6.10 Electrical Sensitivity Features

6.10.1 Electrostatic Discharge (ESD) Electrical Characteristics

Symbol	Parameter	Conditions	Grade
$V_{ESD(HBM)}$	Electrostatic discharge (Human-Body Model HBM)	AEC-Q100-002 Rev-E: 2013	3A

Remark: This specification is guaranteed by the design, and is not tested in mass production.

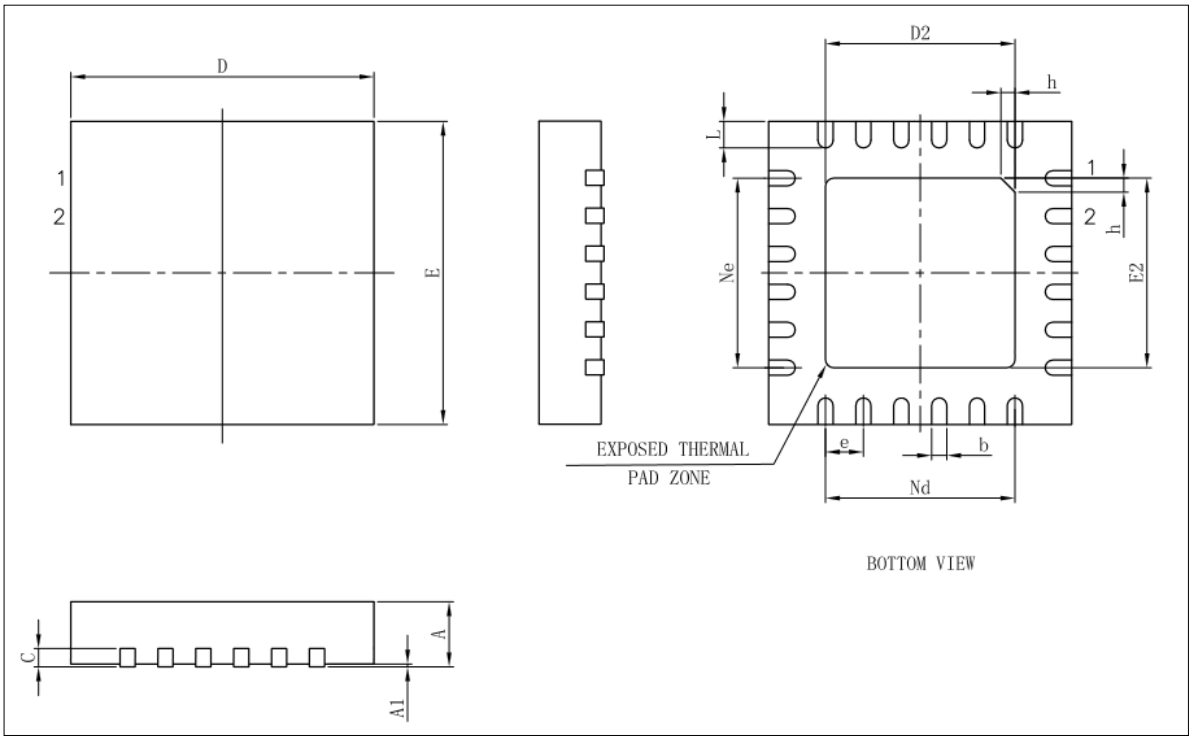
6.10.2 Static Latch-up (LU) Electrical Characteristics

Symbol	Parameter	Conditions	Grade
LU	Static latch-up class	AEC-Q100-004 Rev-D: 2012	Class ⅡA (T_A = 125℃)

Remark: This specification is guaranteed by the design, and is not tested in mass production.

7 Package Information

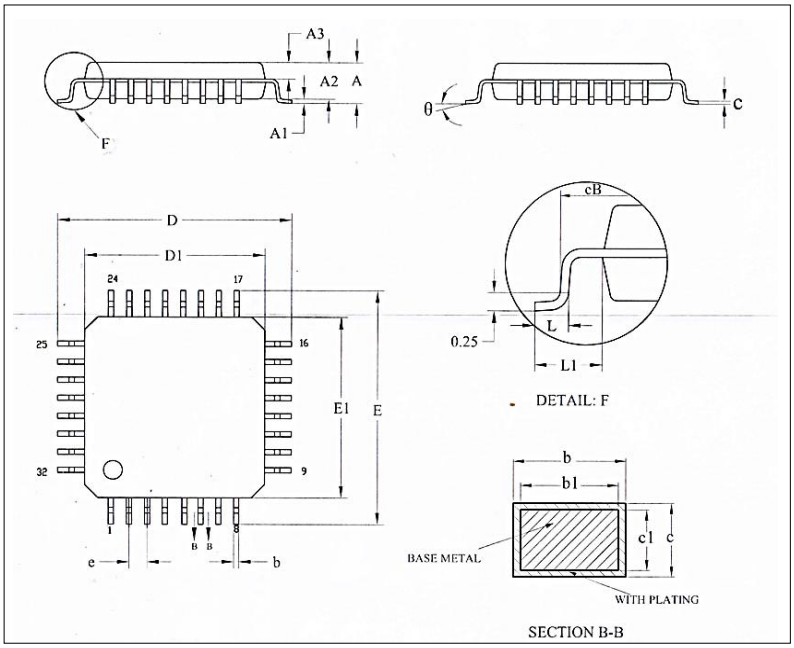
7.1 QFN24 (4x4mm, 0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

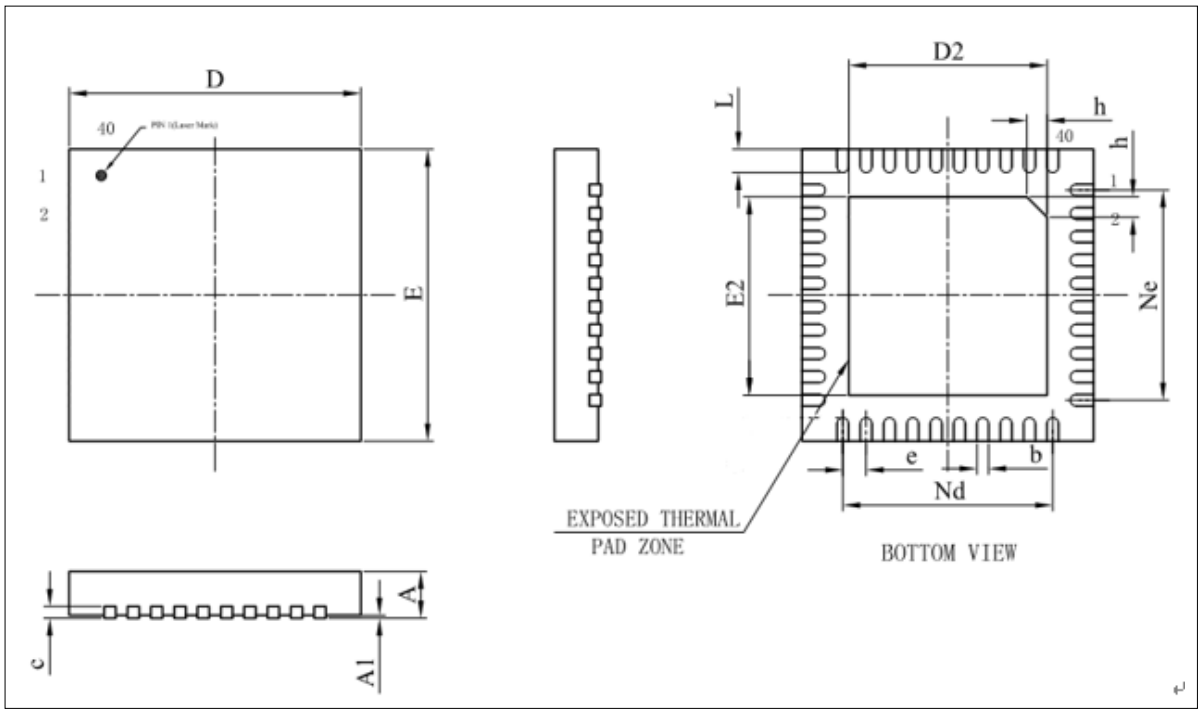
7.2 LQFP32 (7x7mm, 0.8mm)



Symbol	Millimetre		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.41
b1	0.32	0.35	0.38
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

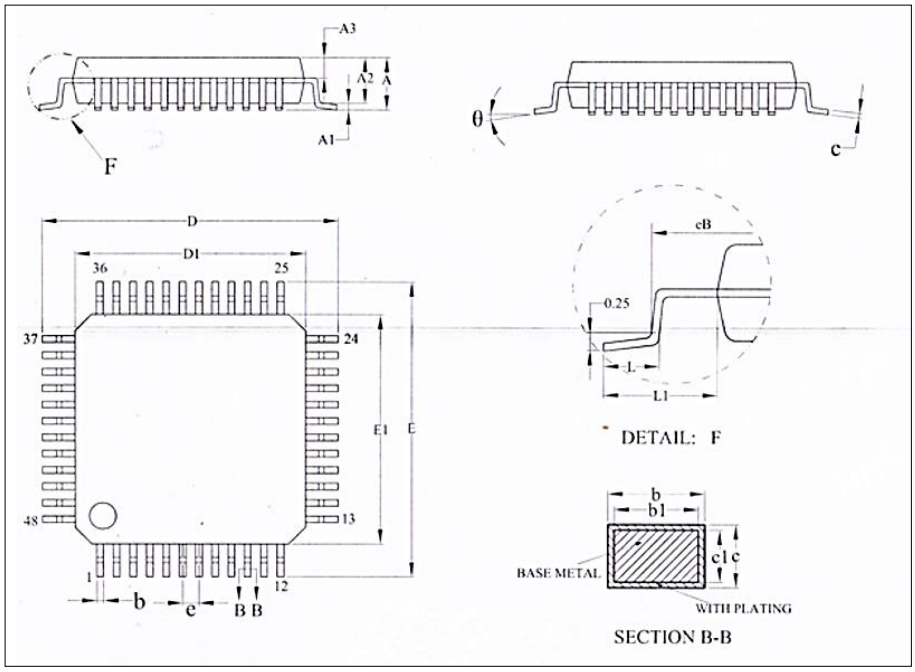
7.3 QFN40 (5x5mm,0.4mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	-	3.80
e	0.40BSC		
Ne	3.60BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	-	3.80
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

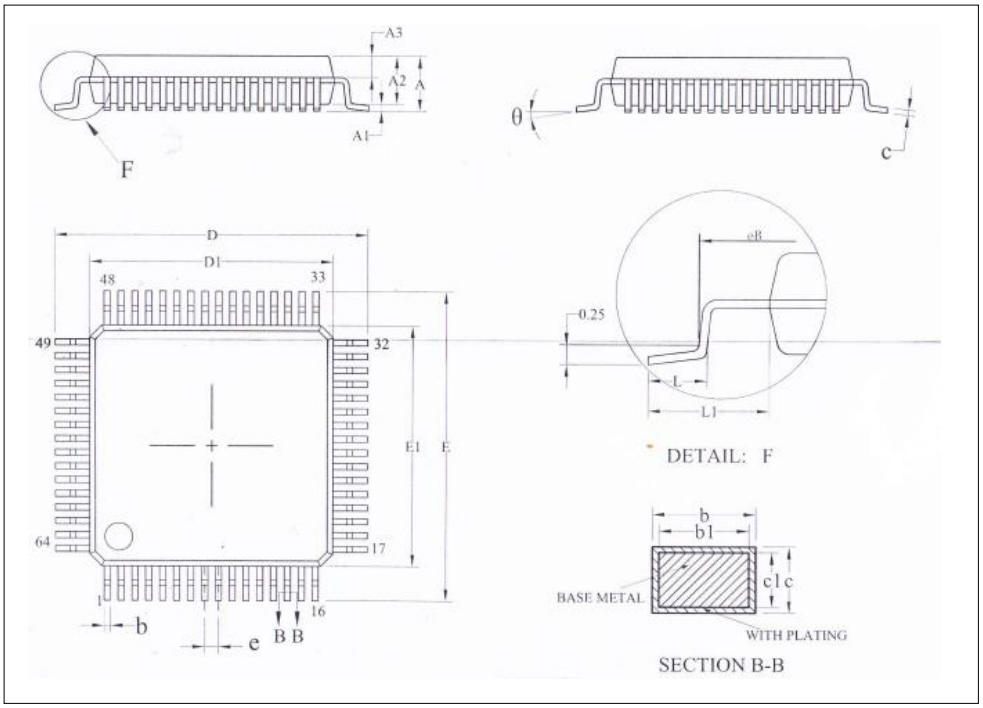
7.4 LQFP48 (7x7mm,0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.43	-	0.75
L1	1.00REF		
θ	0°	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

7.5 LQFP64 (7x7mm, 0.4mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.40BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

8 Version History

Revision	Date	Modify content
V1.00	Feb.2022	Internal First Edition
V1.01	Nov 2022	Modified the parameters in 6.5.1
V1.02	Nov 2022	Modified the function of 32Pin pin in 4.1.2
V1.0.3	Feb 2023	1) Correct some errors in Chapter 1.1; 2) Add notes on parameters for low temperature conditions 3) Correct description of pin function for the product in Chapter 4.1
V1.0.4	Dec 2023	1) Correct some errors in Chapter 5.13.2 2) Update the foot map format 3) Modify the contents of section 6.1/6.4.1 4) Update cover information
V1.0.5	Jan 2024	1) Modified section 6.1 Typical Application Peripheral Circuits 2) Add input current parameters in section 6.3
V1.0.6	Jul 2024	1) Modified QFN24/QFN40/LQFP48 package dimensions 2) Modified the parameters in section 6.9.1/6.10 3) Modified the Electrical Sensitivity Features
V1.0.7	Oct 2024	1) Revised the cover page 2) Delete incorrect content in the function description
V1.0.8	June.2025	Delete section 5.26 with errors